

JIWA1/A2

Schematics Document

Mobile Penryn uFCPGA Intel Cantiga_GM/PM+ICH9-M

Wednesday, May 14, 2008

REV:1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

POWER SEQUENCE

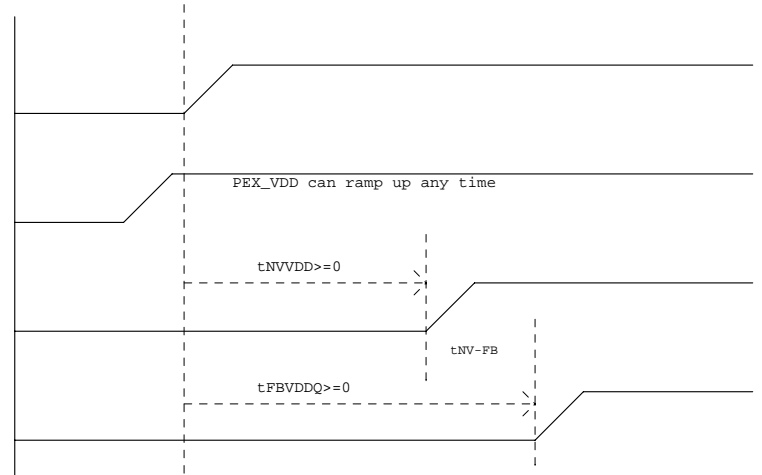
The ramp time for any rail must be more than 40us

(+3VS) VDD33

(1.1VS) PEX_VDD

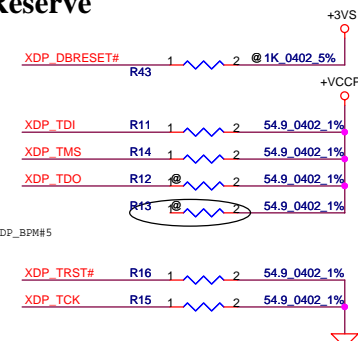
(+VGA_CORE) NVVD

(1.8VS) FBVDDQ

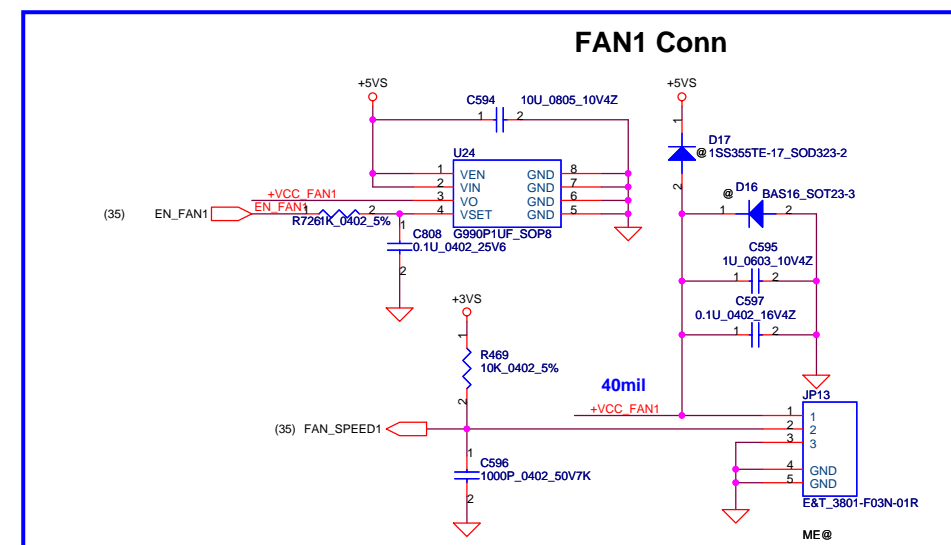
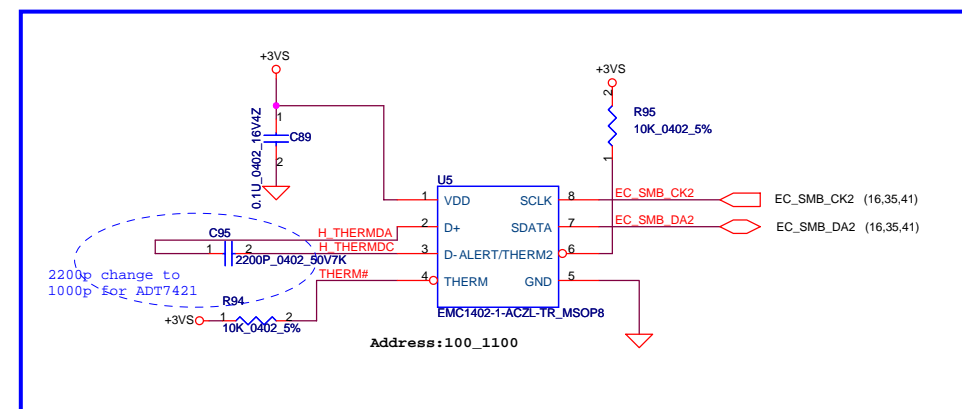


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XDP Reserve



reserved by XDP_BPM#5

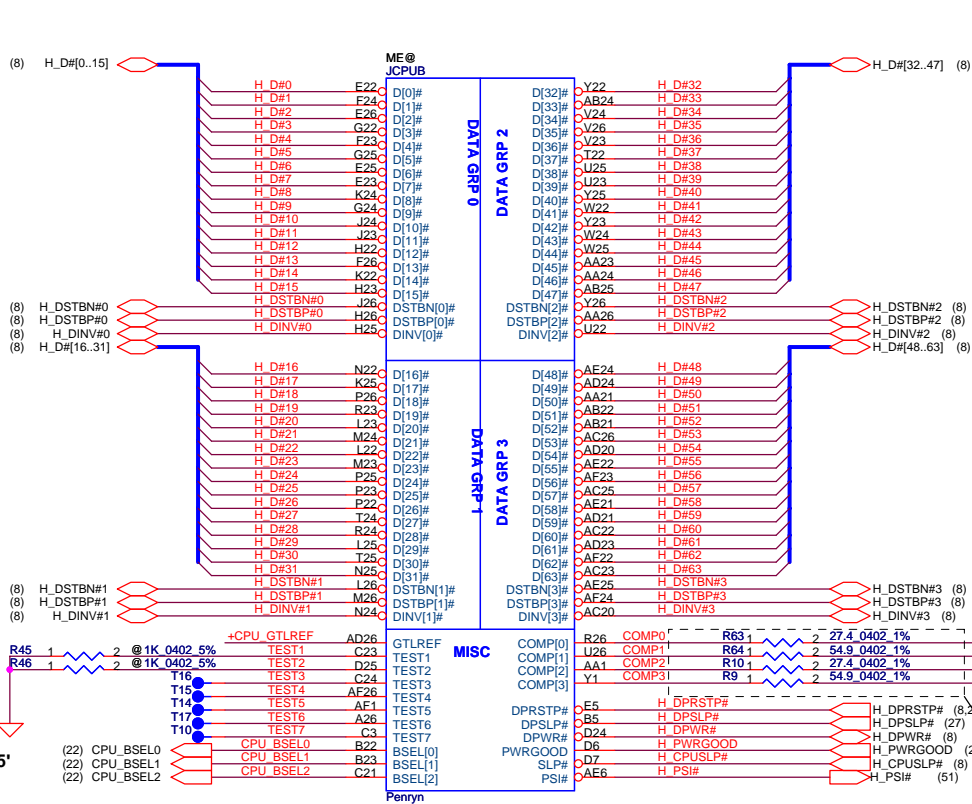


**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

RSVD pins on the CPU
should be left as NO
CONNECT

Penryn

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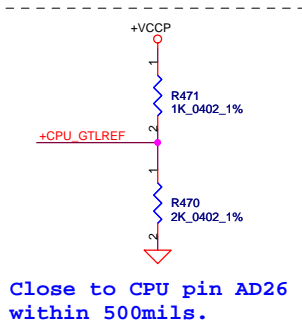
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)

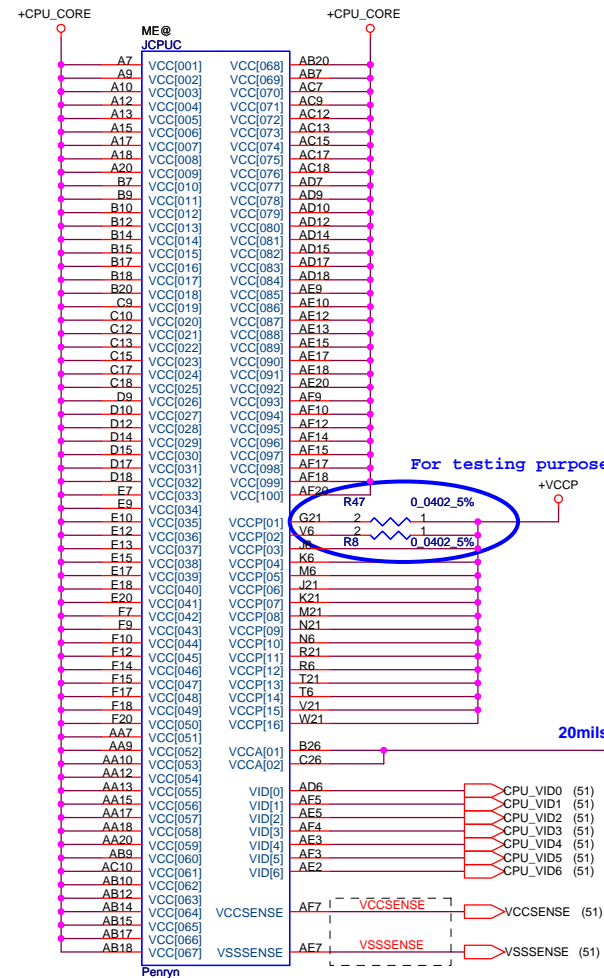
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

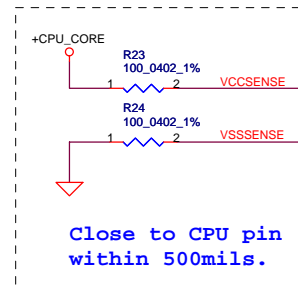


Layout note: Z0=55 ohm
0.5" max for GTLREF.

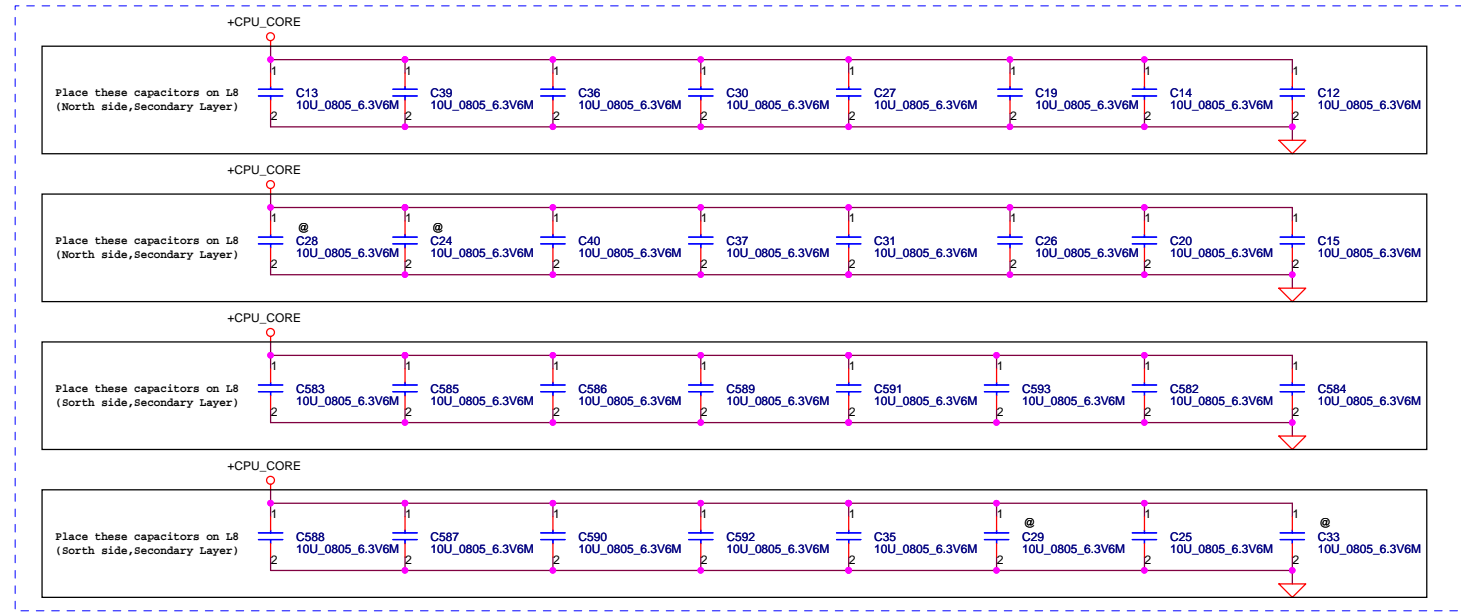
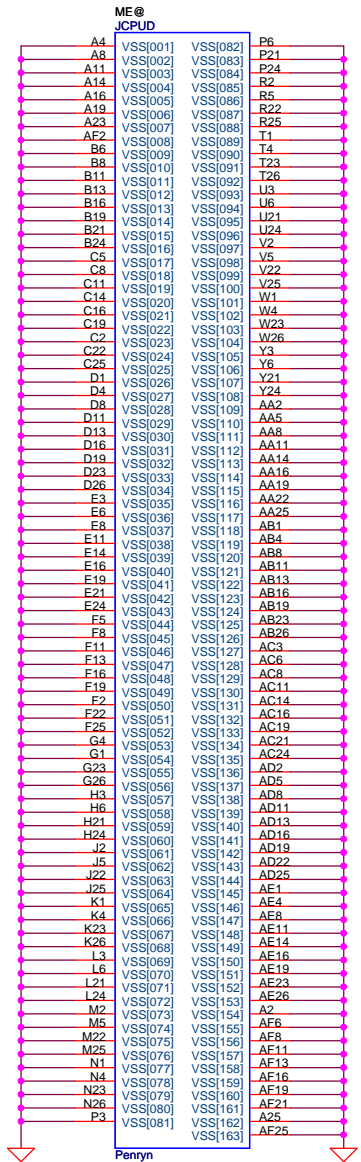


Length match within 25 mils.
The trace width/space/other is
16/7/25.

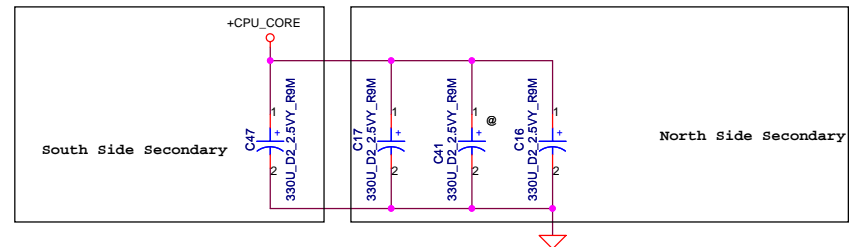
Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



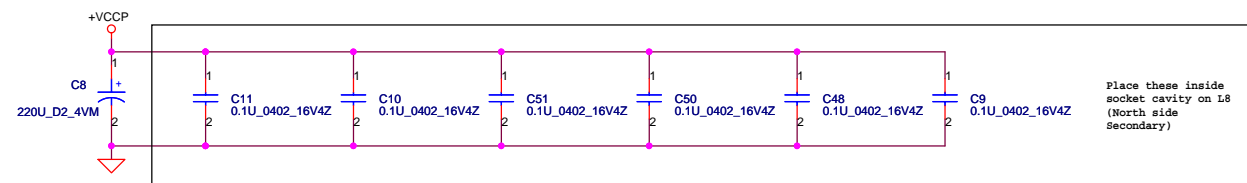
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Mid Frequency Decoupling

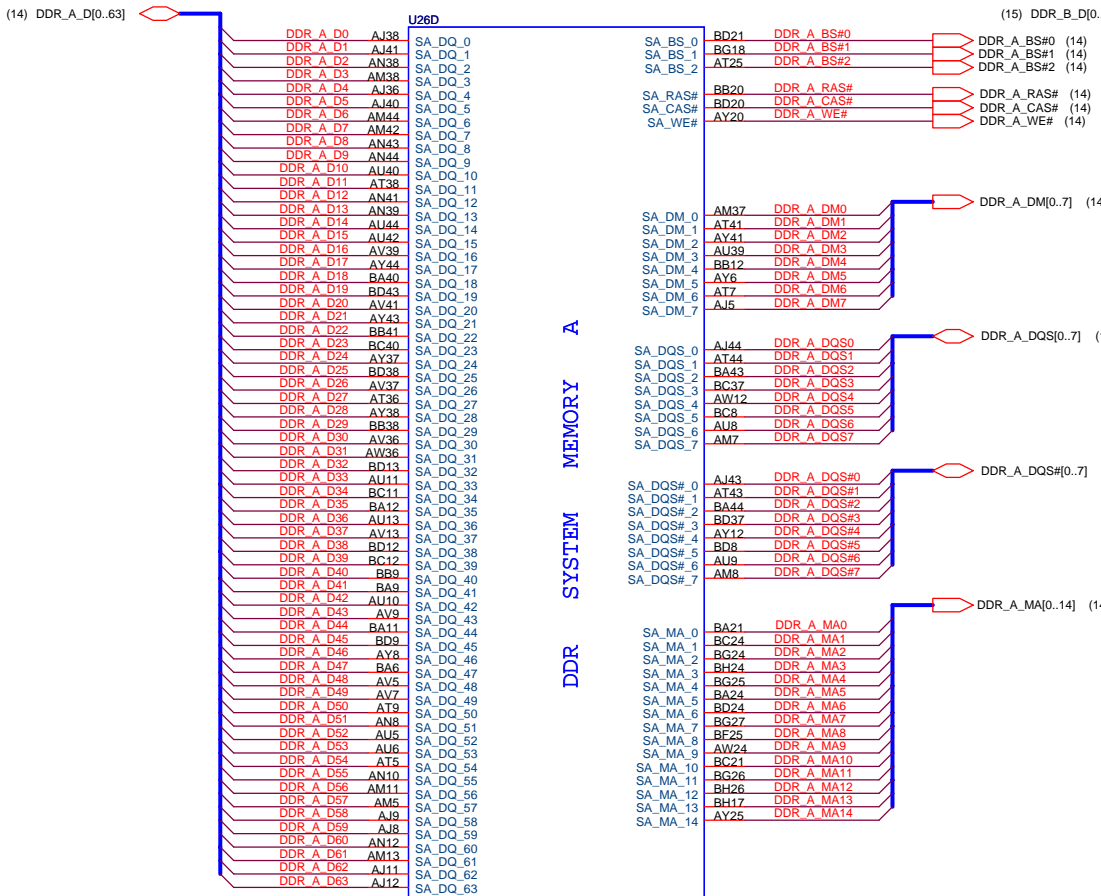


ESR <= 1.5m ohm
Capacitor > 1980uF



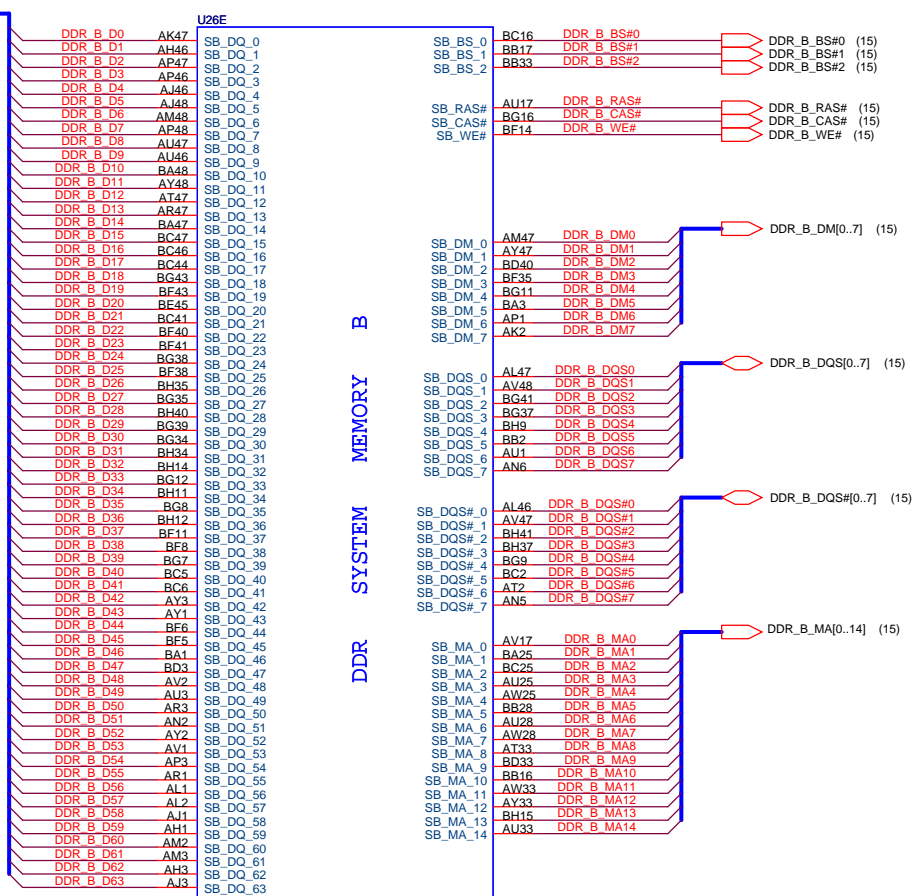
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(14) DDR_A_D[0..63]



GM@

(15) DDR_B_D[0..63]

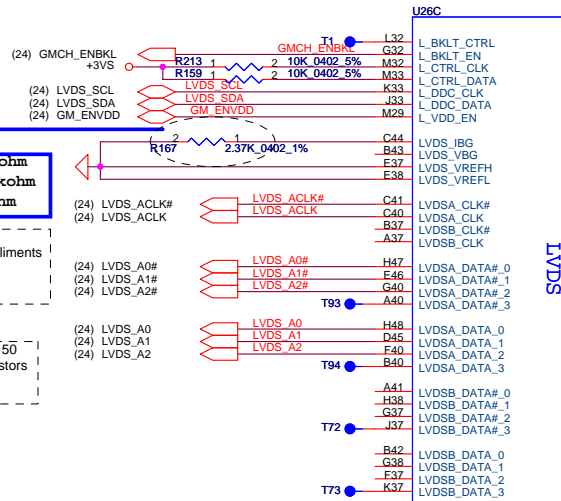


GM@

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2008/10/15		2008/10/15		Cantiga GMCH (2/6)-DDRII	
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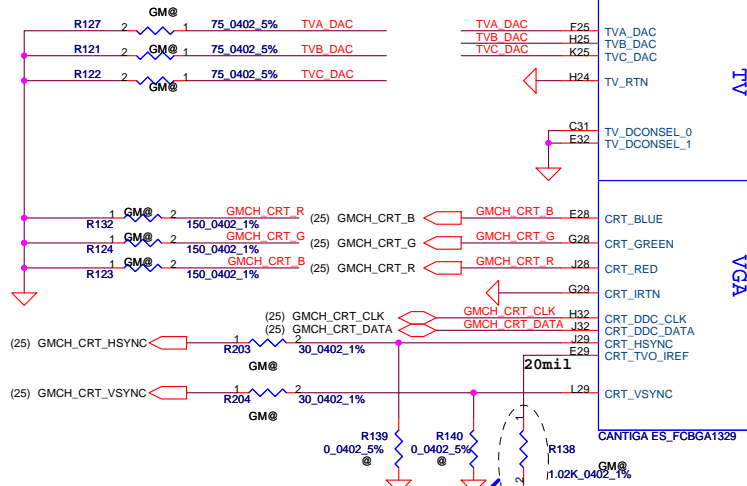
Please check Power source if want support IAMT



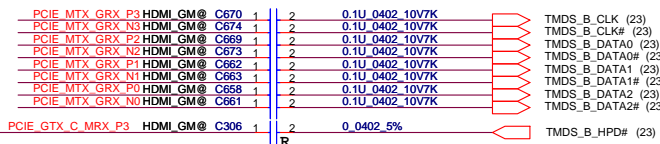
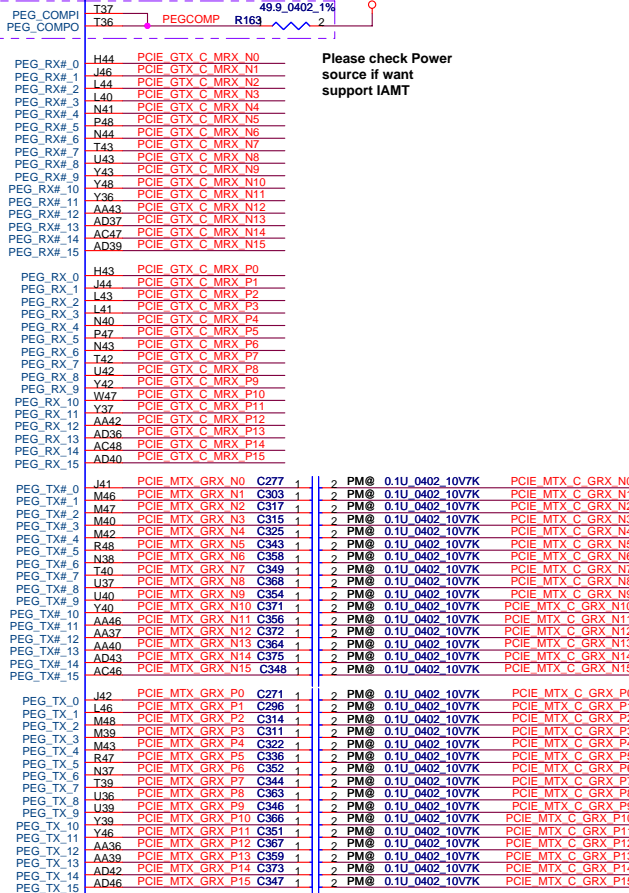
For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5Kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

Layout Note: Place 150 Ohm termination resistors close to GMCH

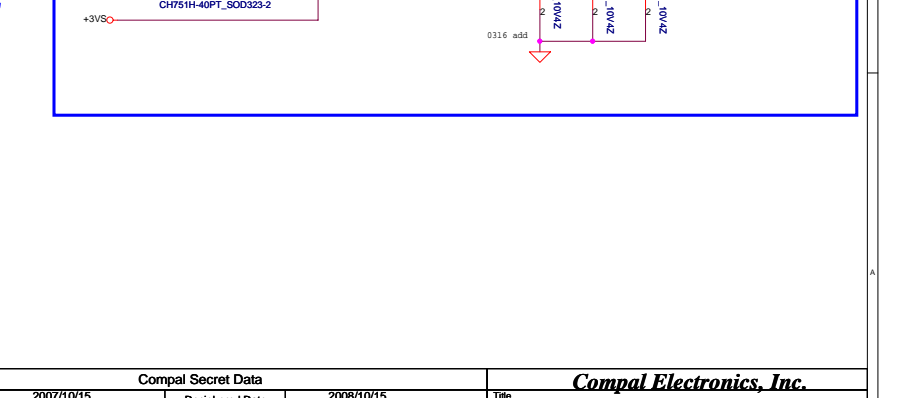
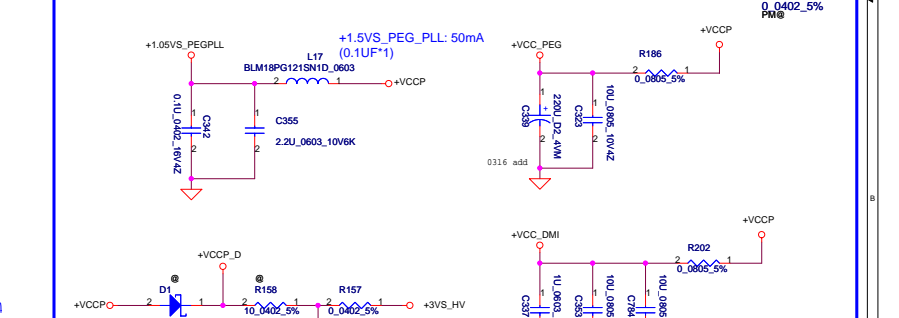
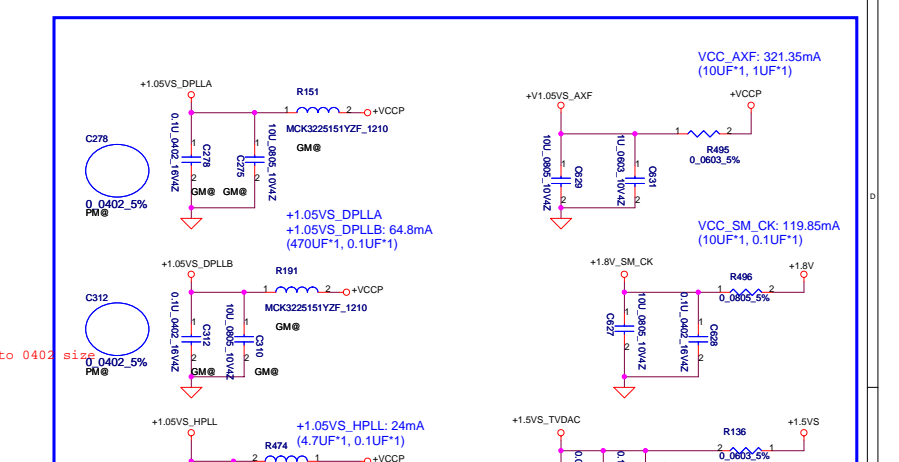
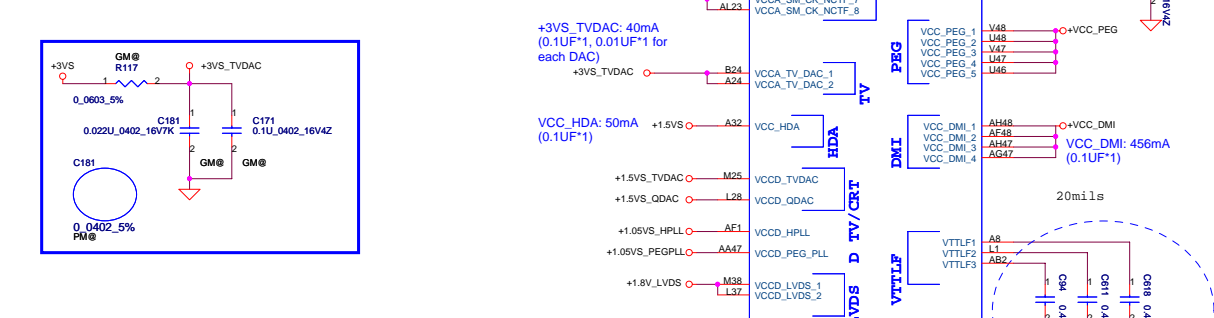
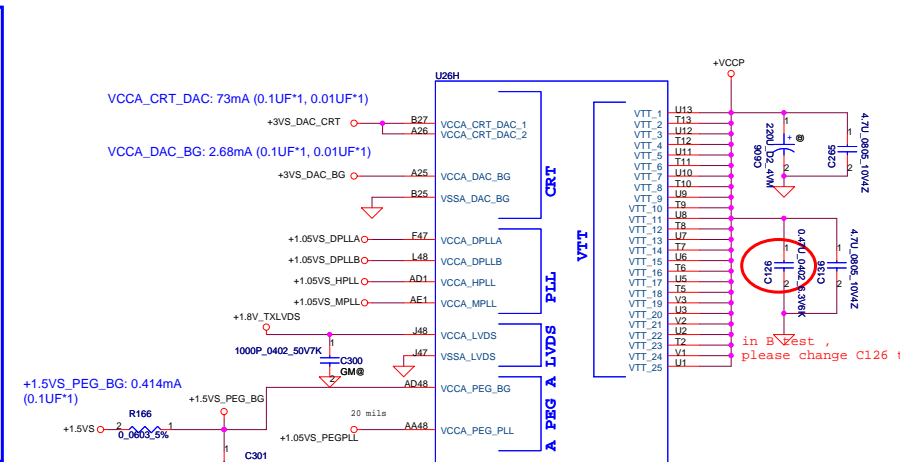


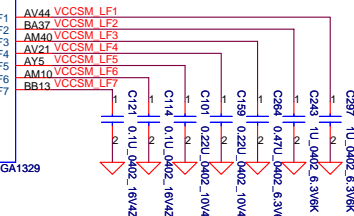
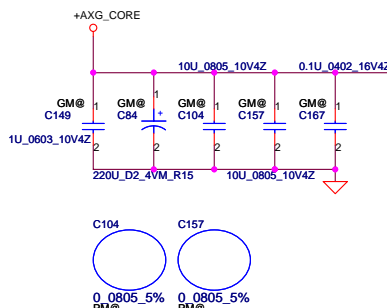
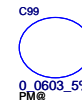
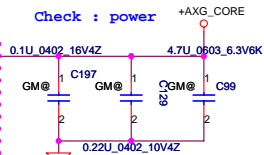
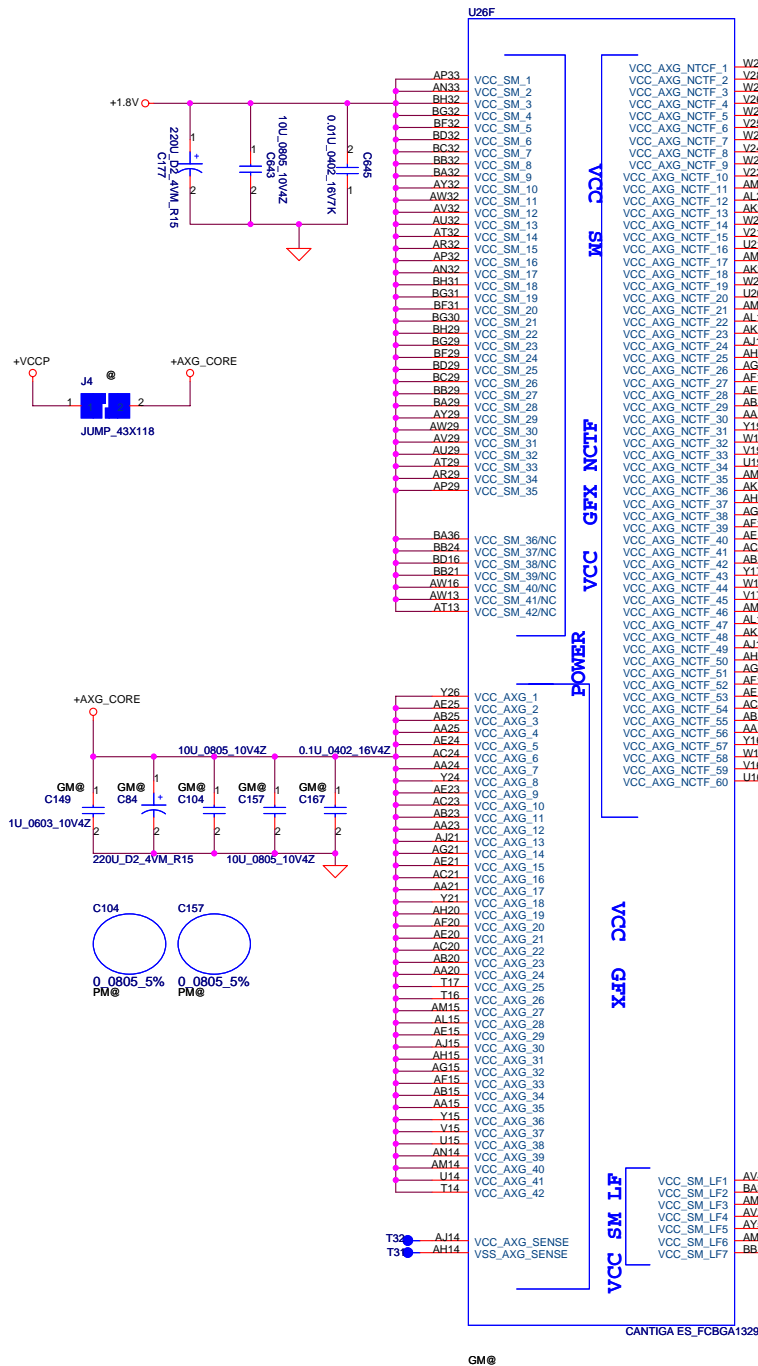
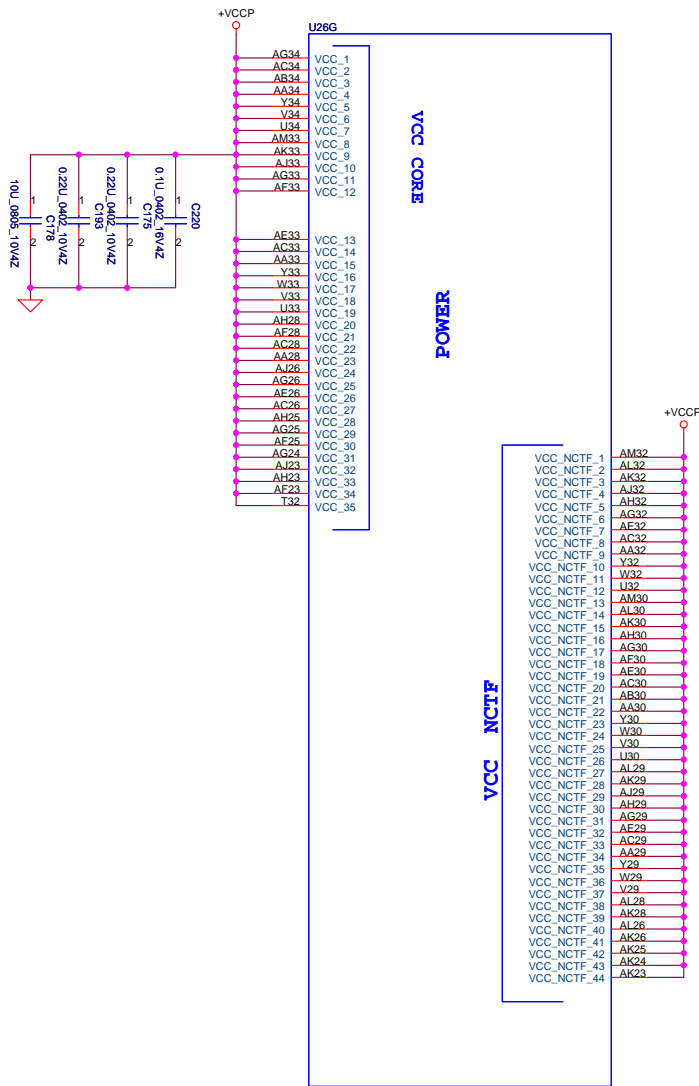
For Cantiga:1.02kohm
For Crestline:1.3kohm
For Calero: 255ohm



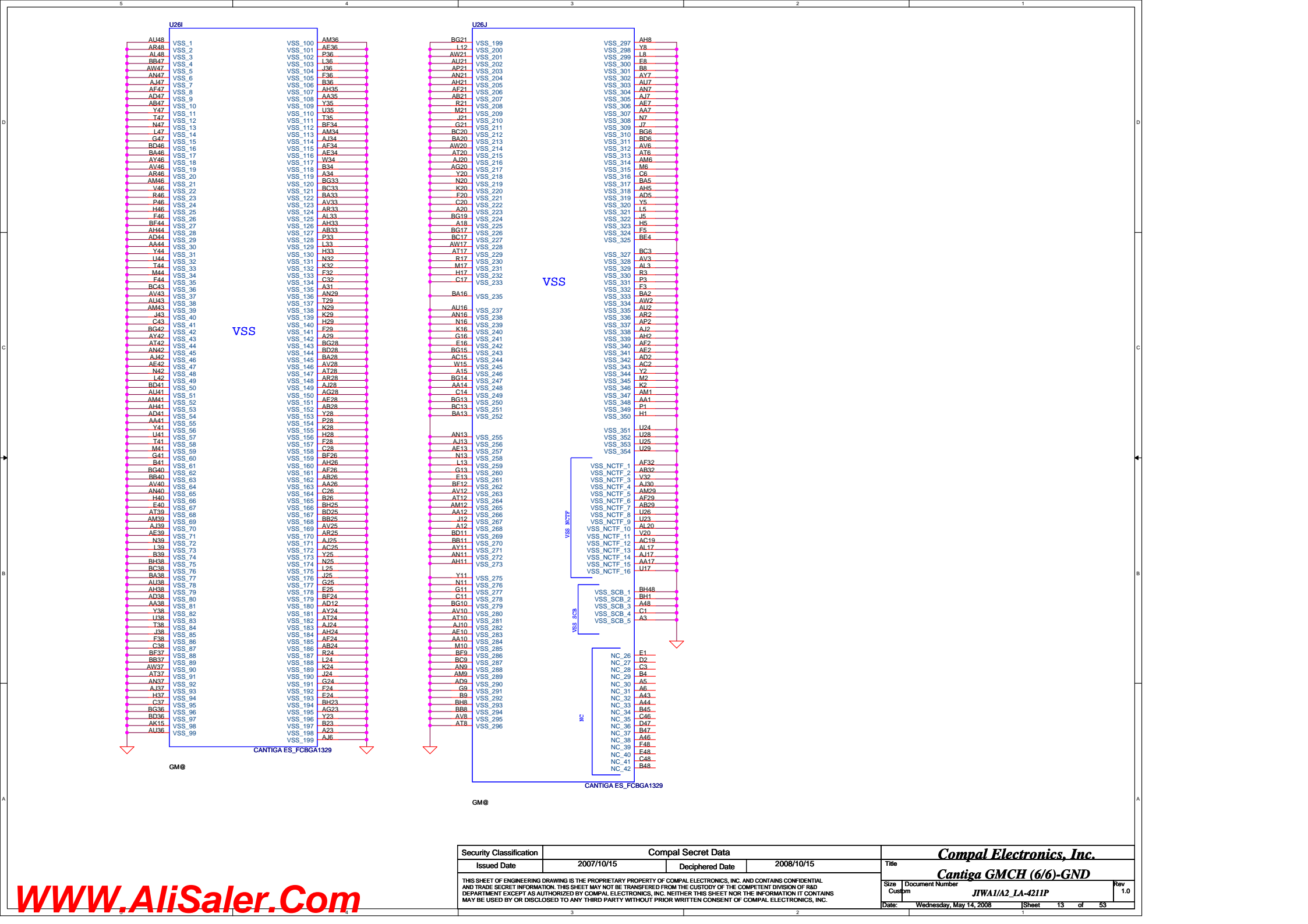
Strap Pin Table

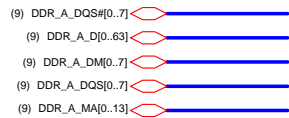
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chipser suite with no confidentiality 1 =(TLS)chipser suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



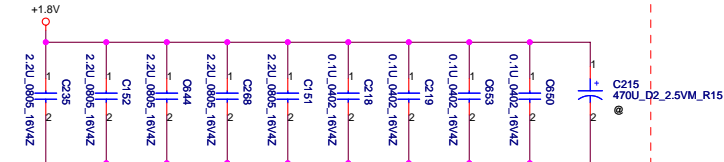


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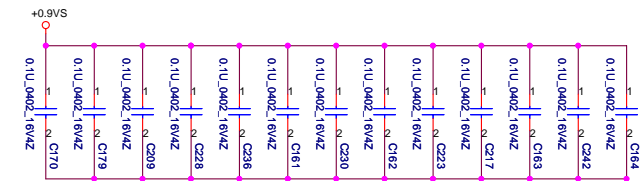




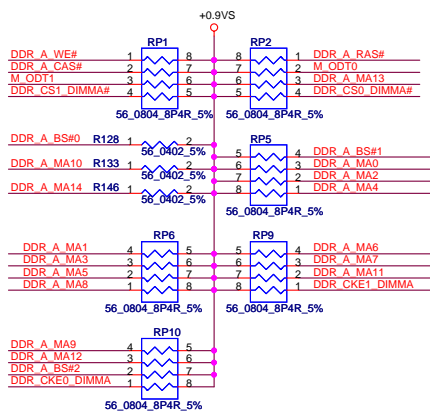
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

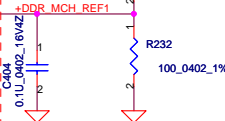


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.

(15) +DDR_MCH_REF1



(15,35,37) EC_TX_P80_DATA

(8) DDR_CKE0_DIMMA

(15,35,37) EC_RX_P80_CLK

(9) DDR_A_BS#2

(9) DDR_A_BS#0

(9) DDR_A_WE#

(9) DDR_A_CAS#

(8) DDR_CS1_DIMMA#

(8) M_ODT1

(8) M_ODT1

(8) M_ODT1

(8) M_ODT1

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(8) M_ODT1

(8) M_ODT1

(8) M_ODT1

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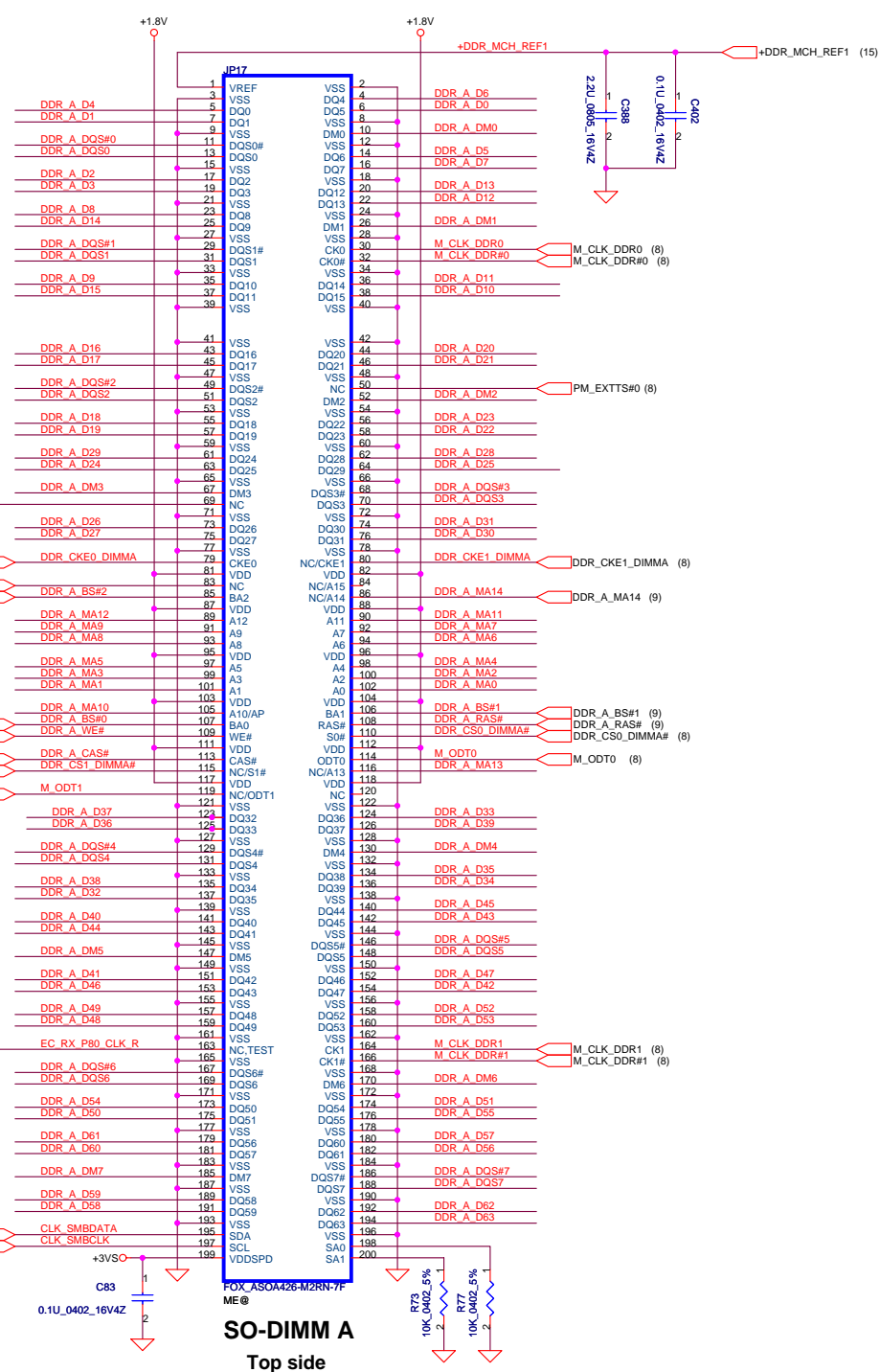
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(8) M_ODT1

(8) M_ODT1

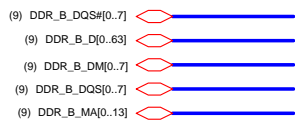
(8) M_ODT1

(8) M_ODT1

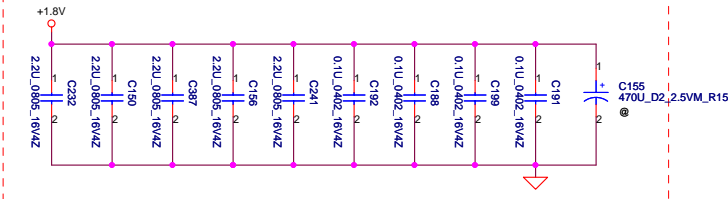


SO-DIMM A
Top side

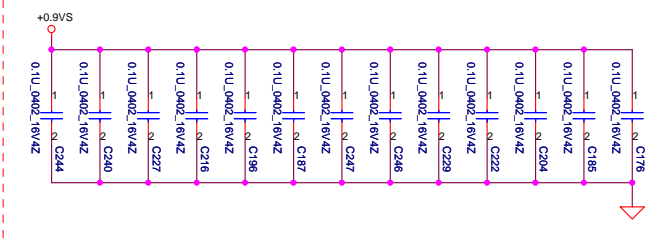
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								DDRII-SODIMM SLOT1			
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						Custom		JTWAI/A2_1A-4211P		1.0	
Date:						Monday, May 12, 2008		Sheet		14 of 53	



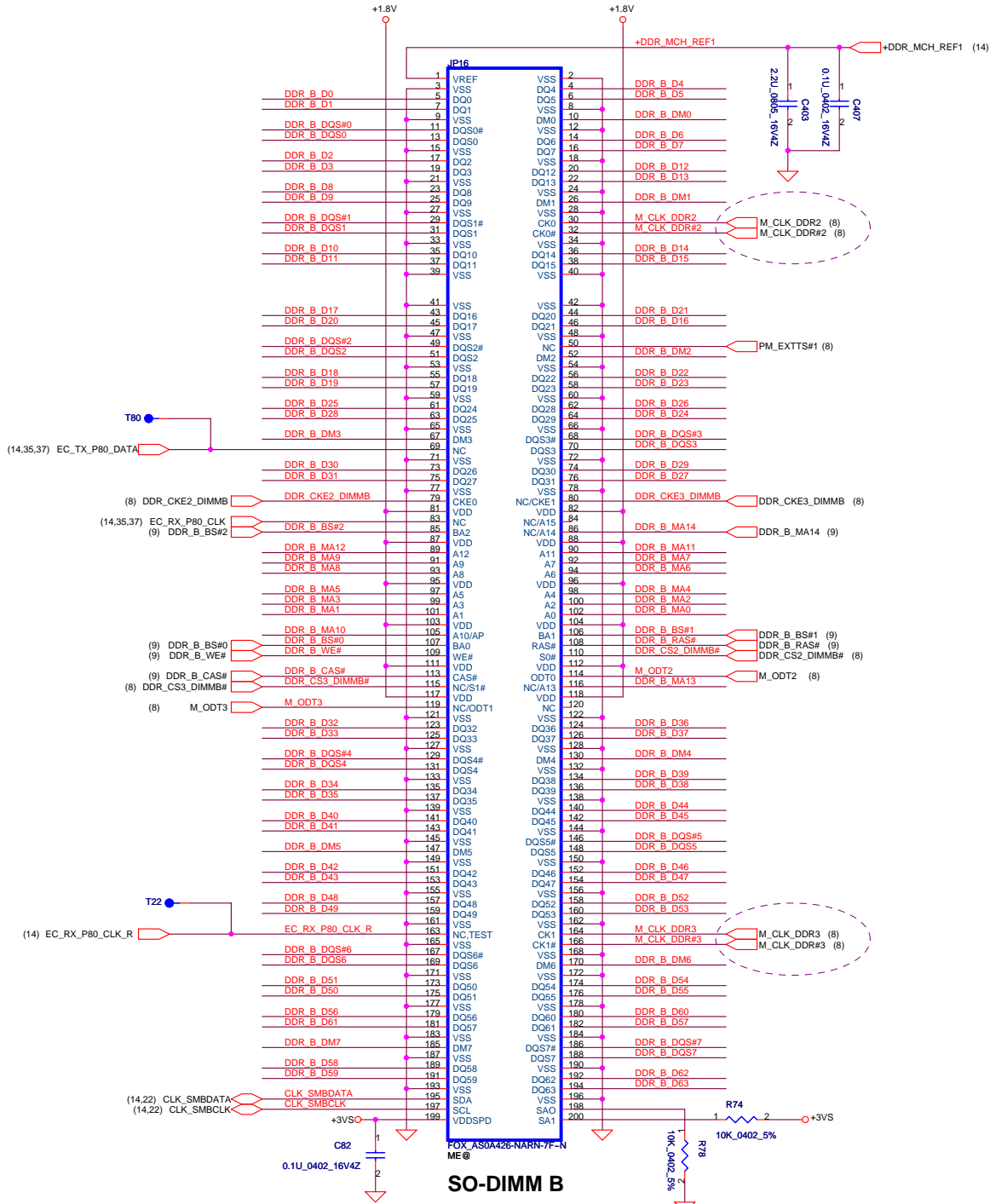
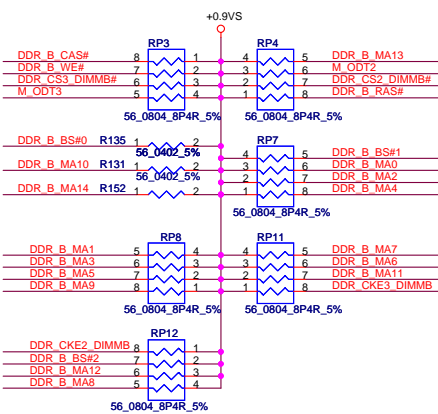
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

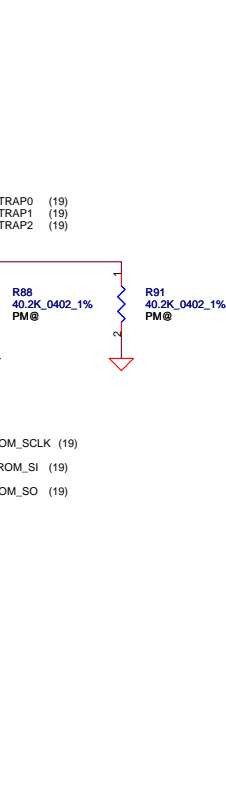
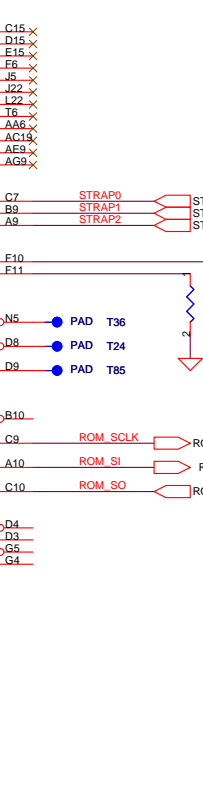
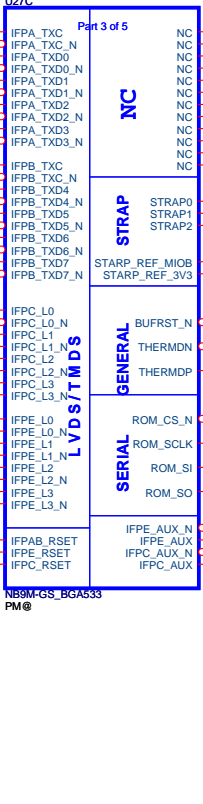
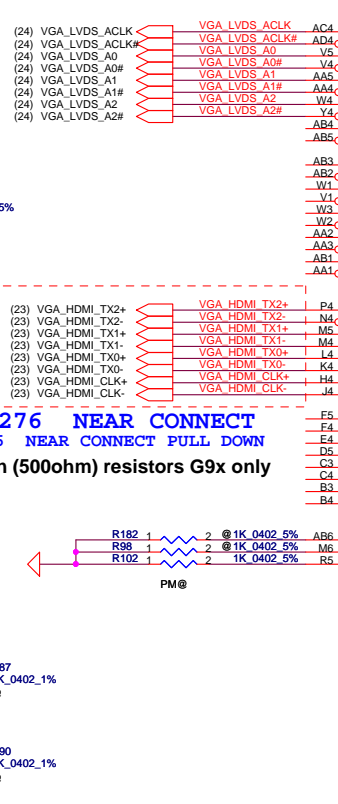
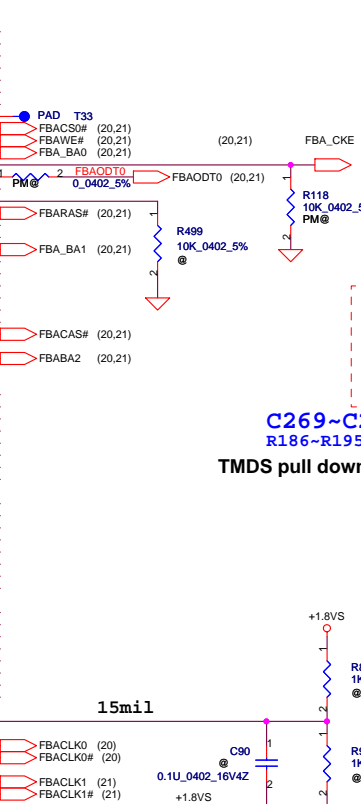
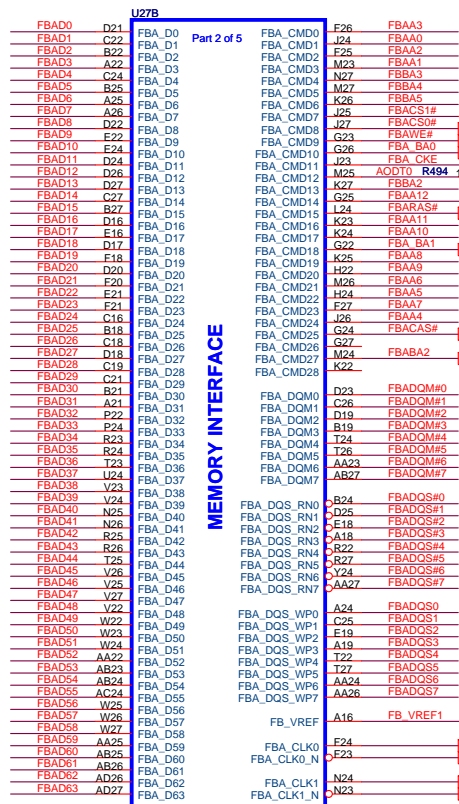
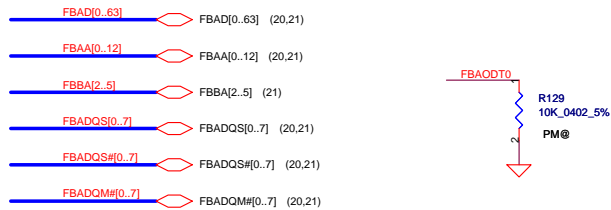


Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"

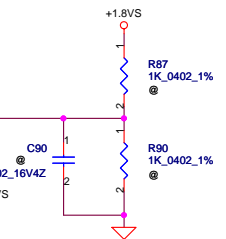


SO-DIMM B

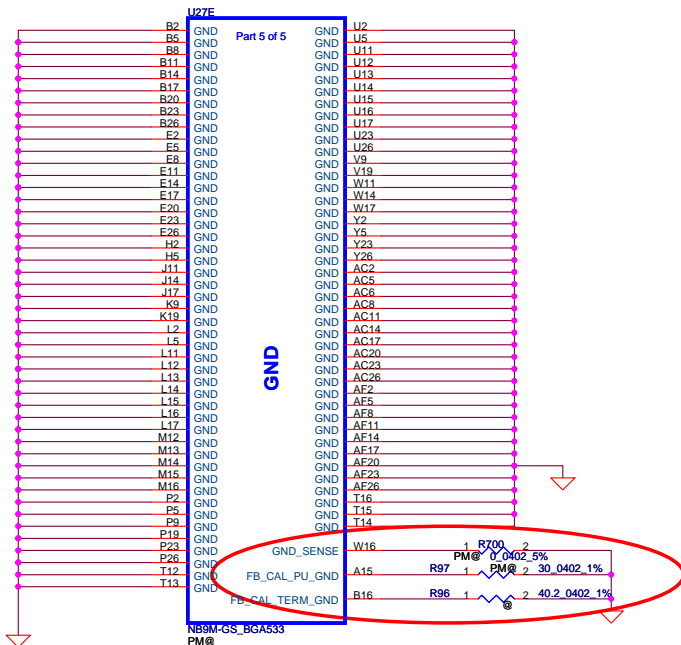
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Issued Date				2007/10/15				2008/10/15			
Deciphered Date											
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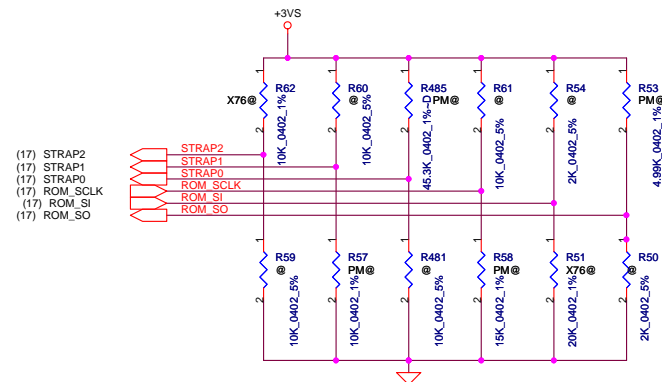
C269~C276 NEAR CONNECT
 R186~R195 NEAR CONNECT PULL DOWN
 TMDs pull down (500ohm) resistors G9x only



Security Classification		Compal Secret Data		Title	
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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available

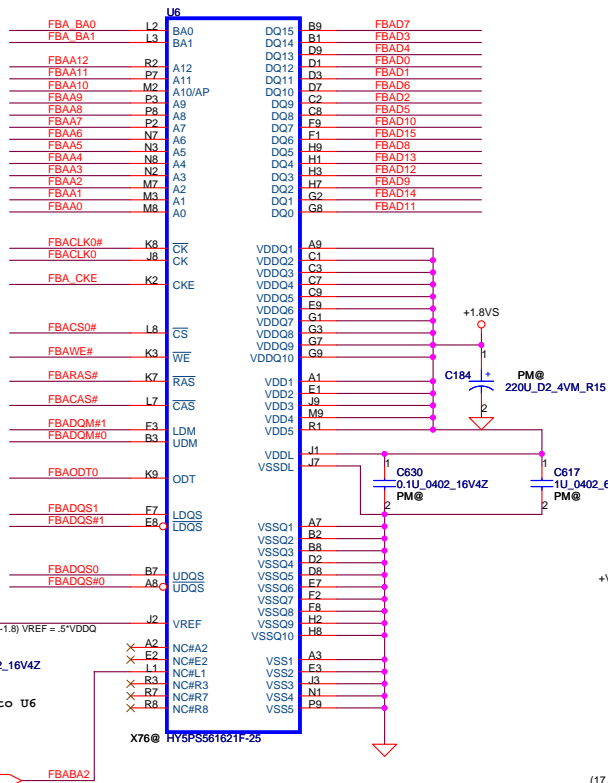


GB1 Family GPU Strap Options

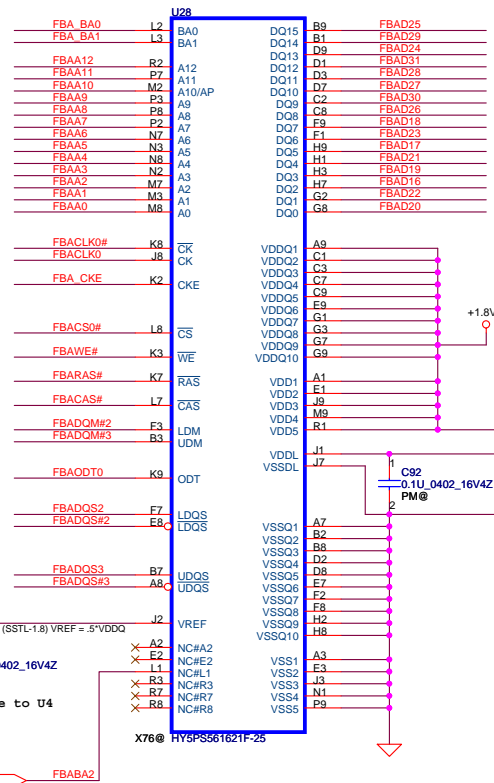
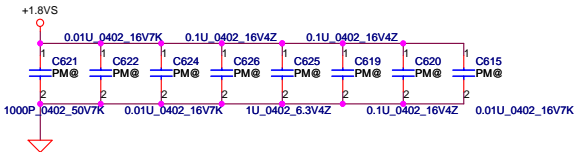
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 10K	PD 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 10K	PD 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 10K	PD 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 45K
NB9M-GE (0x06E8)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PU 5K	PD 45K
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PU 5K	PD 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PU 5K	PD 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PU 5K	PD 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PU 5K	PD 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PU 5K	PD 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (16M*16)	Hynix	SA000012G30	X7611338L01
	Qimonda	SA00001YF10	X7611338L02
	Samsung	SA00001KH10	X7611338L03
DDR2 VRAM (32M*16)	Hynix	SA00000FF30	X7611338L04
	Qimonda	SA00000S820	X7611338L05
	Samsung	SA00001VX10	X7611338L06

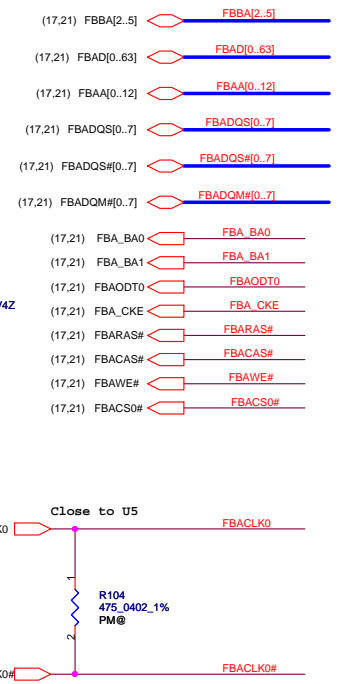
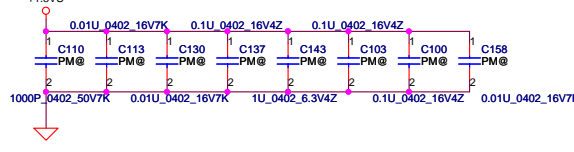
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	NB9M-GE GND & STRAP		
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				Date: Monday, May 12, 2008	Sheet 19 of 53	

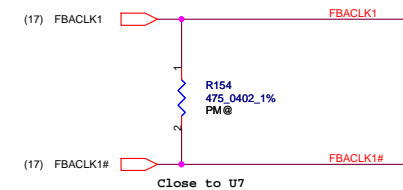
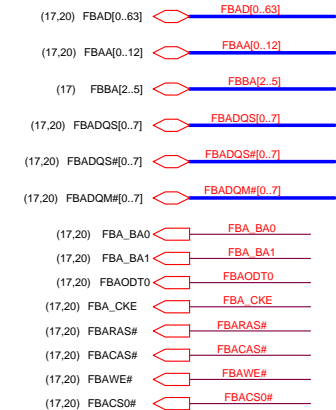
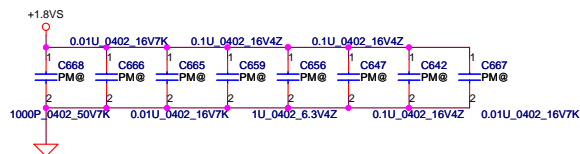
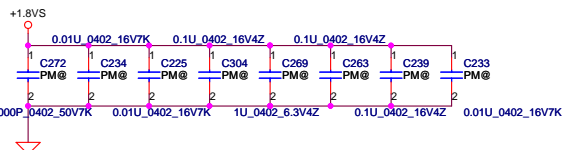


DDR2 BGA MEMORY



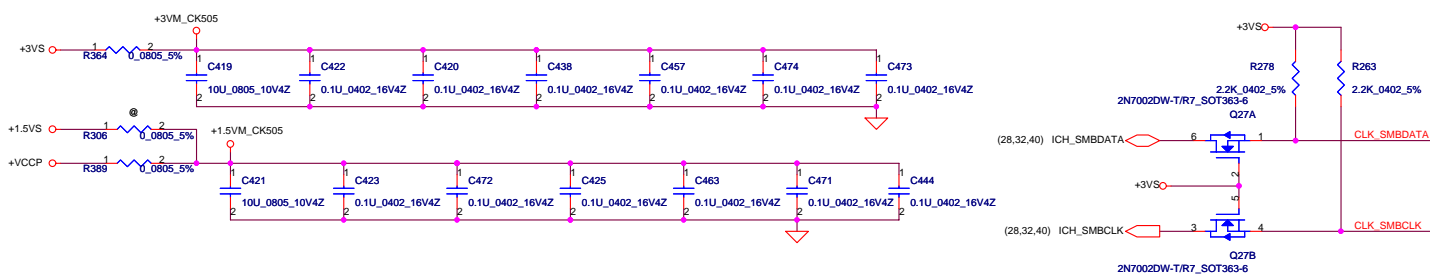
DDR2 BGA MEMORY



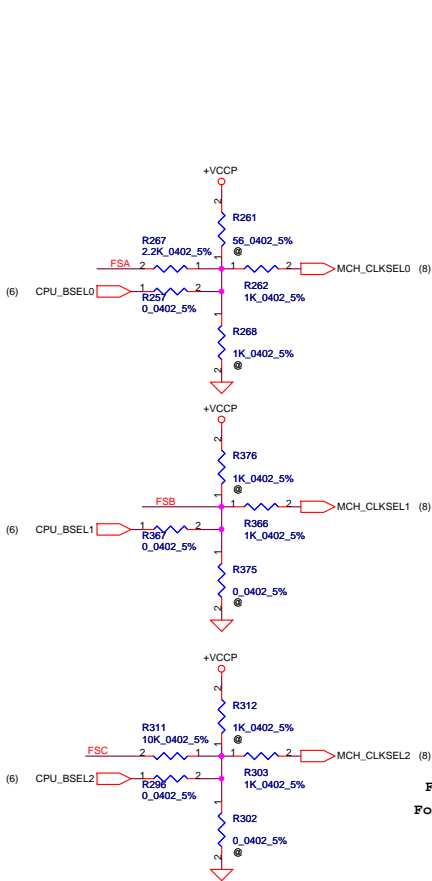


Security Classification		Compal Secret Data		Compal Electronics, Inc. VRAM DDRB	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Document Number	1.0
				Custom J1WAI/A2_LA-4211P	
Date: Monday, May 12, 2008				Sheet	21 of 53

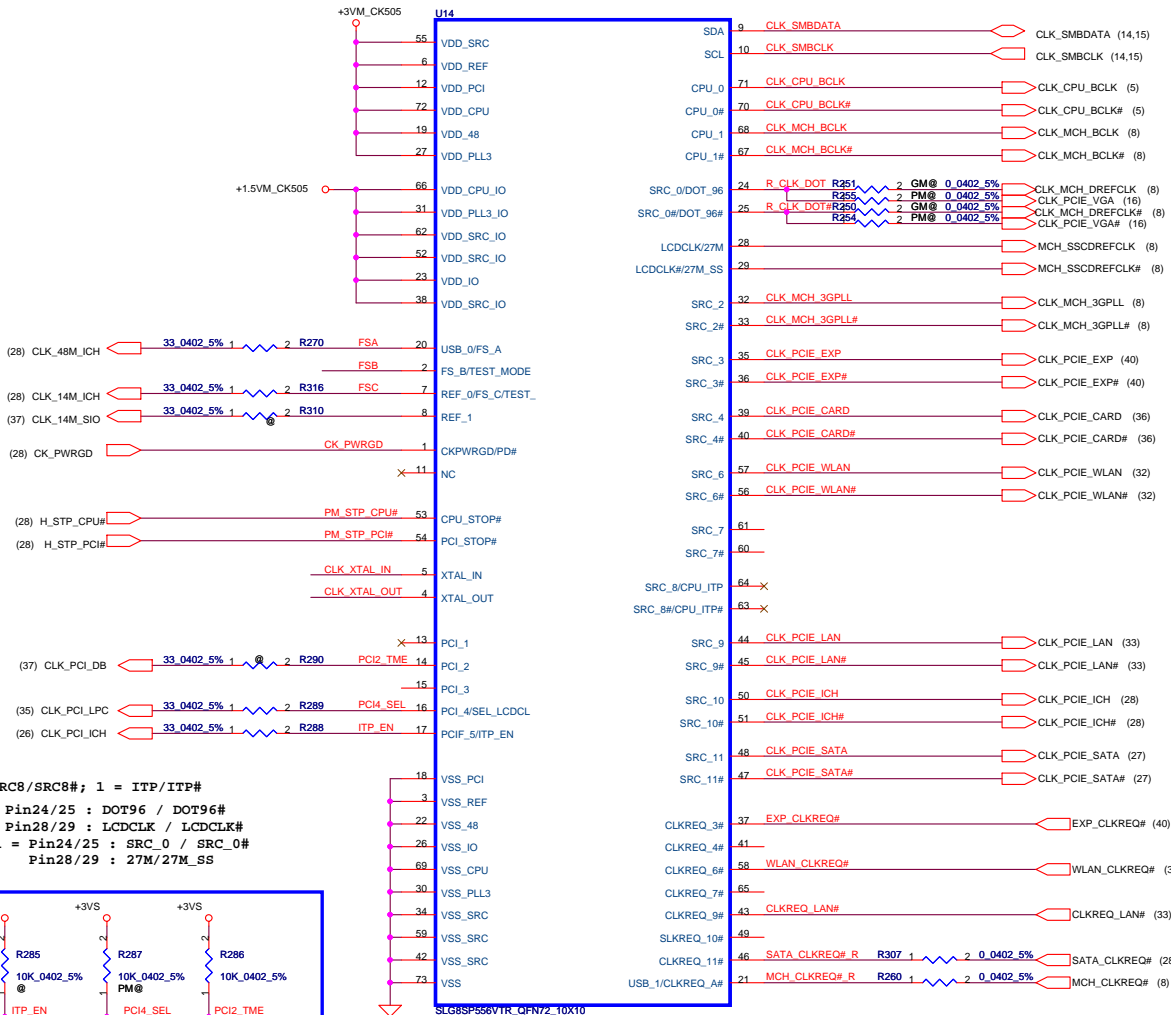
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Compal Electronics, Inc.

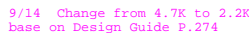
Clock generator

J1W1A2_LA-4211P

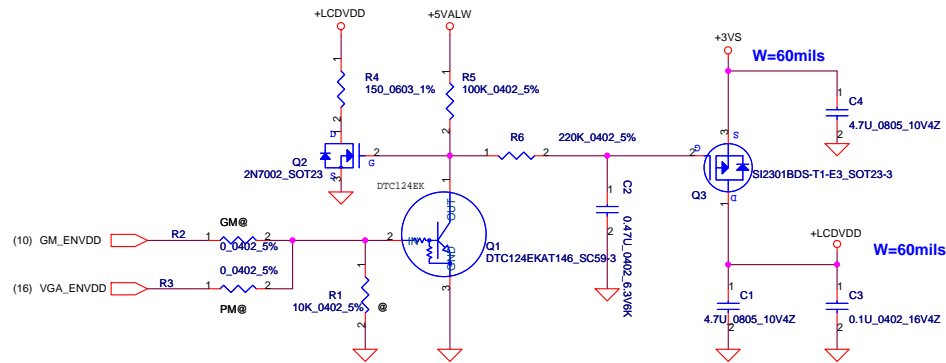
Monday, May 12, 2008 Sheet 22 of 53

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				Rev 1.0

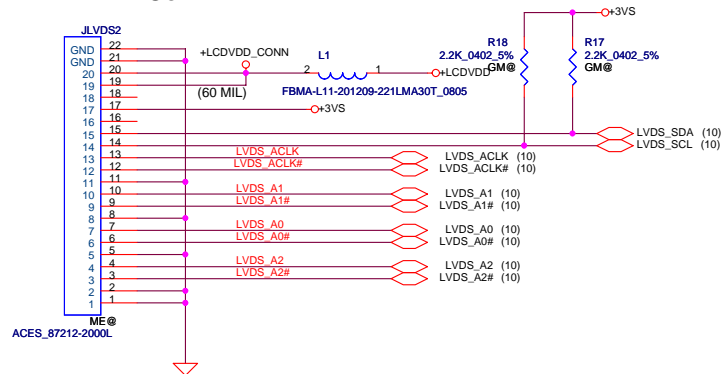
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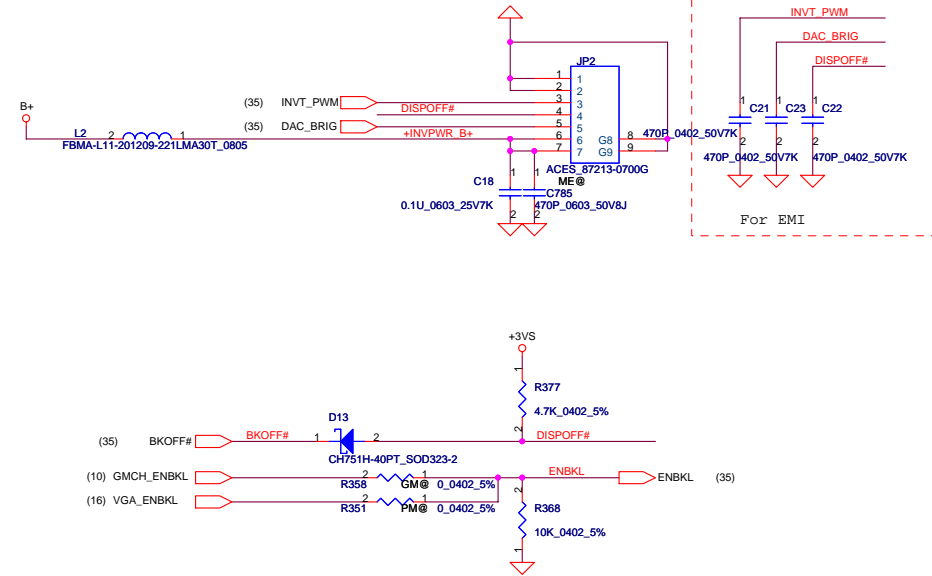
LCD POWER CIRCUIT



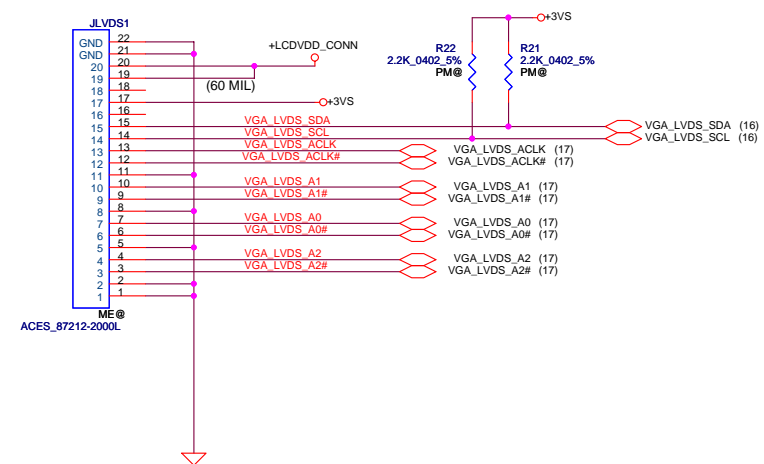
LCD/PANEL BD. Conn.



INVERTER Conn.



LCD/PANEL BD. Conn.



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					Size B	Document Number	JIWAI/A2 LA-4211P	Rev 1.0
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Compal Electronics, Inc.

LVDS & DVI Connector

J1W1/A2_LA-4211P

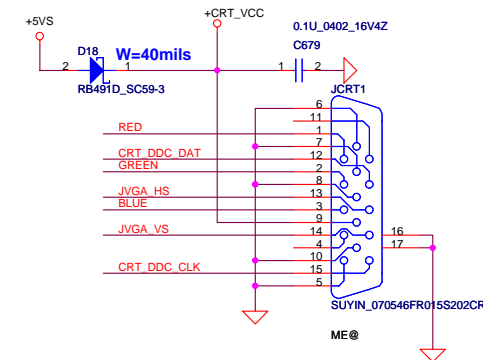
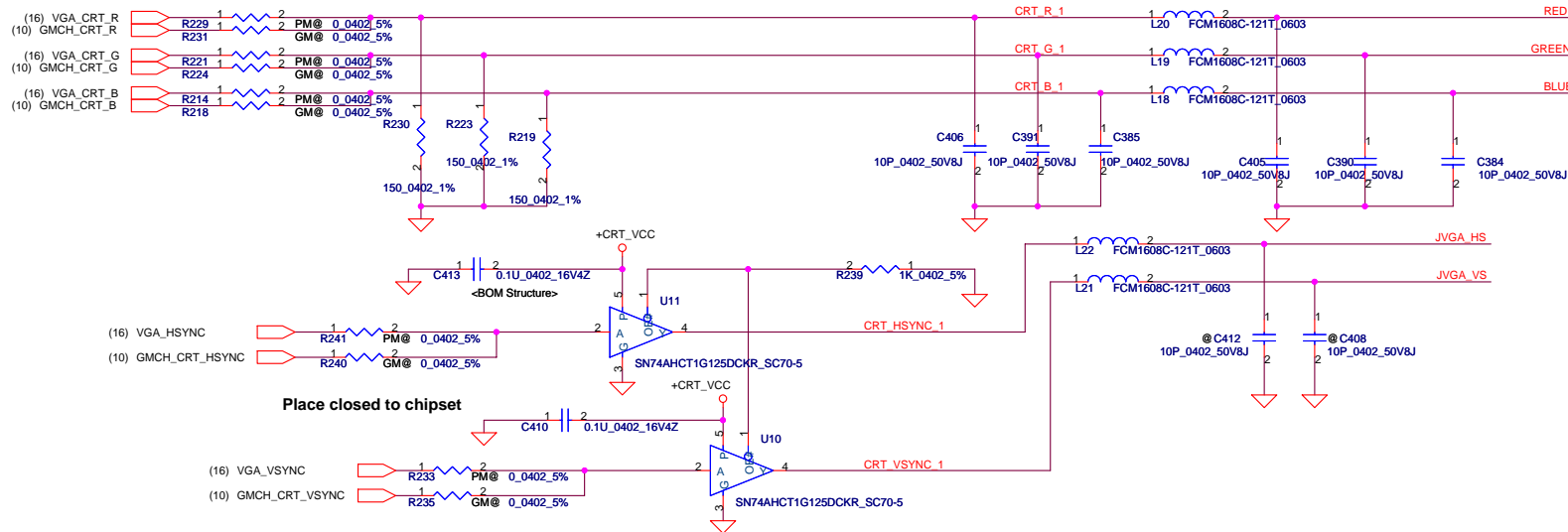
Rev 1.0

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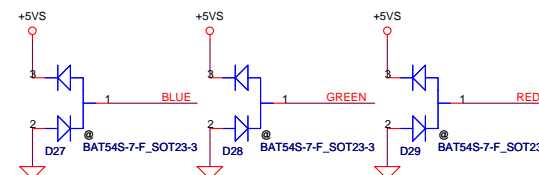
CRT Connector

Place closed to chipset

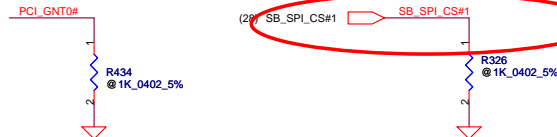
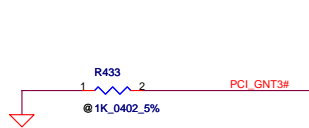
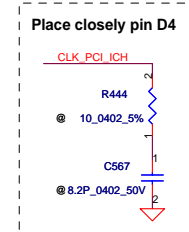
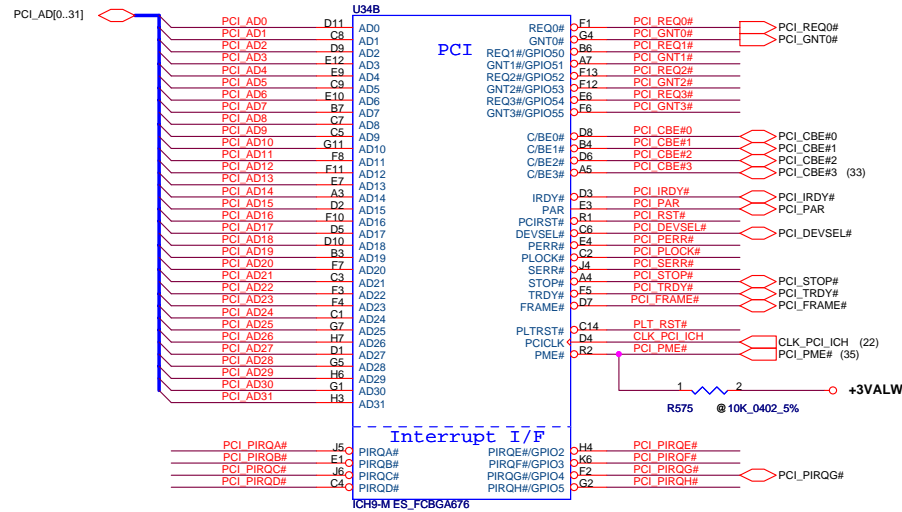
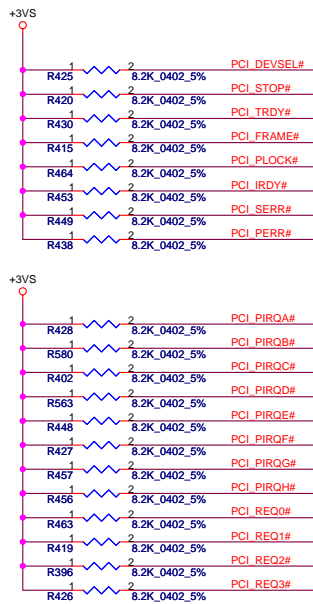


PIN ASSIGMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4



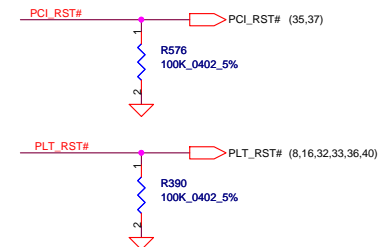
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	Rev		1.0
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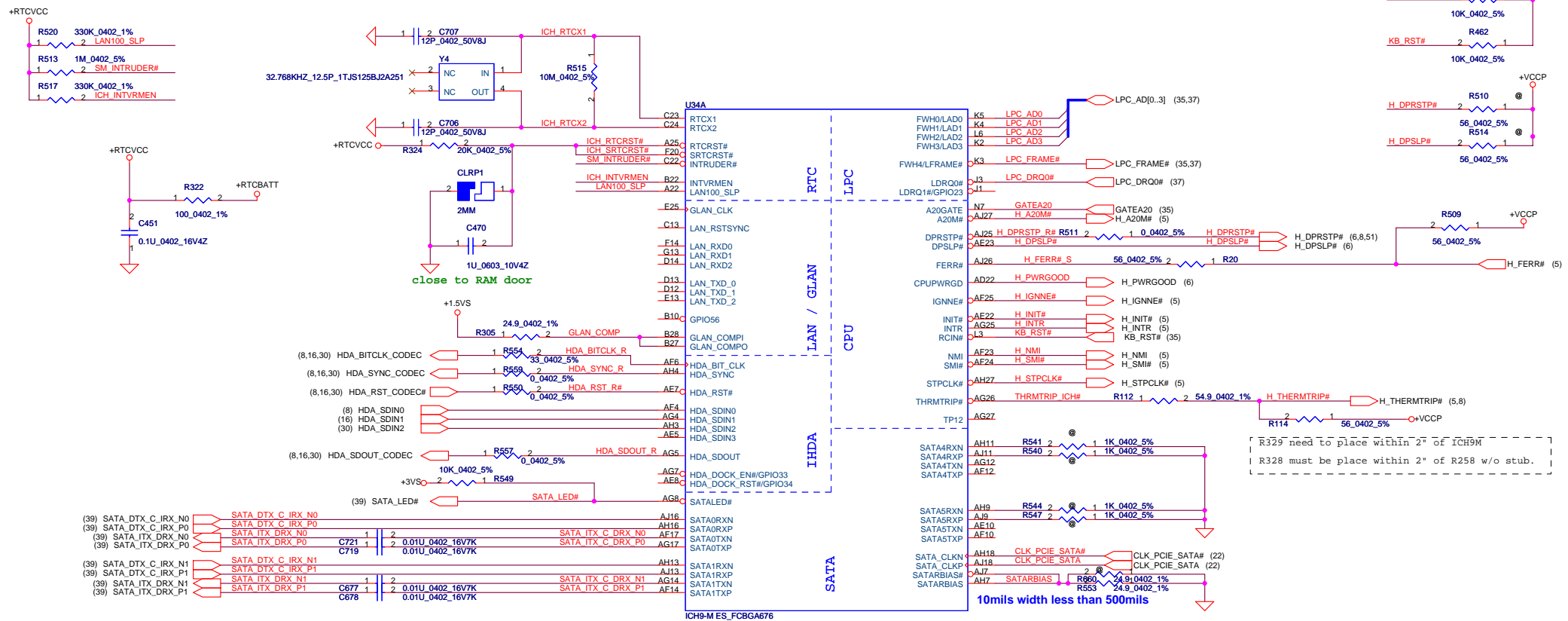


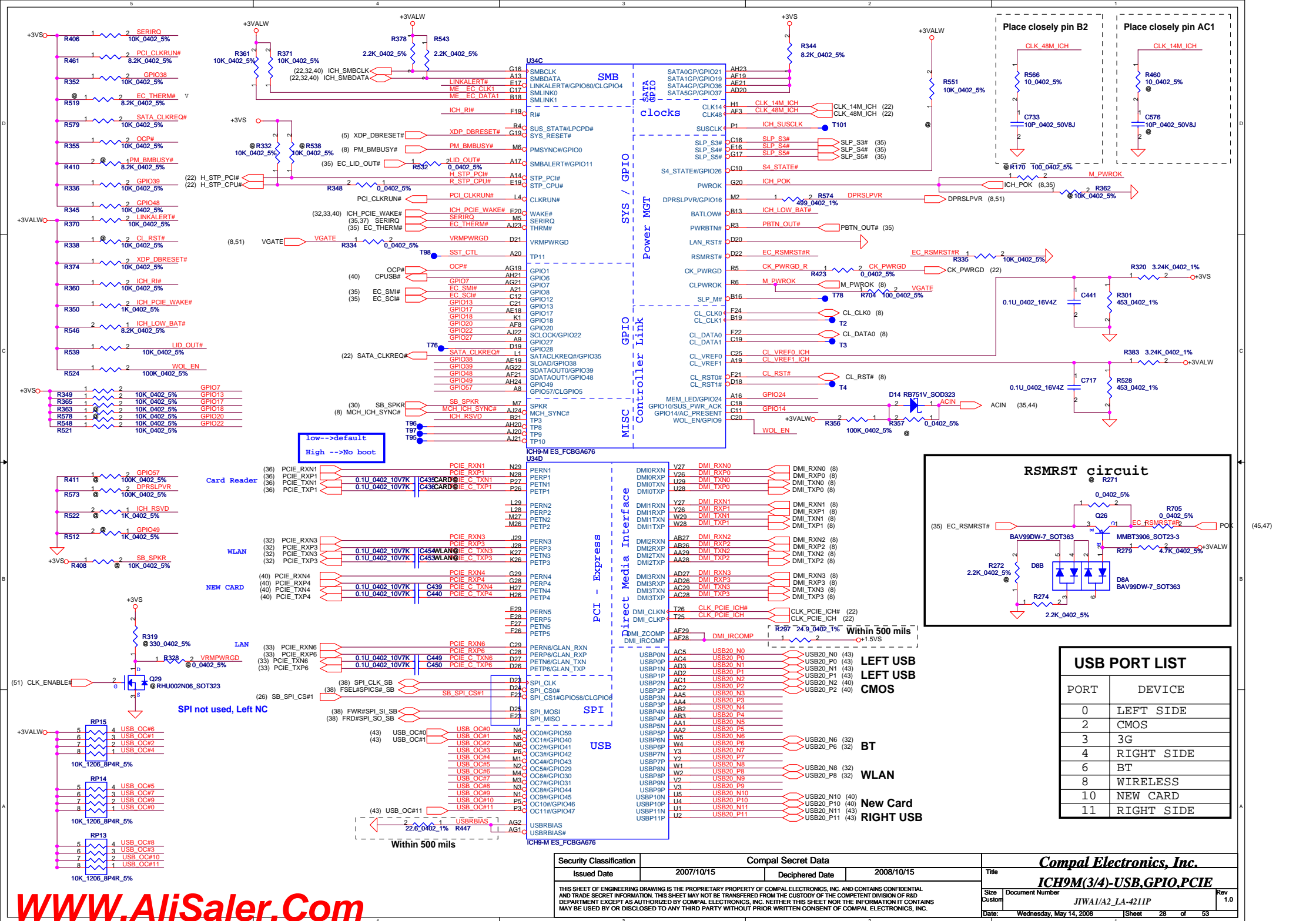
Pull high?

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*







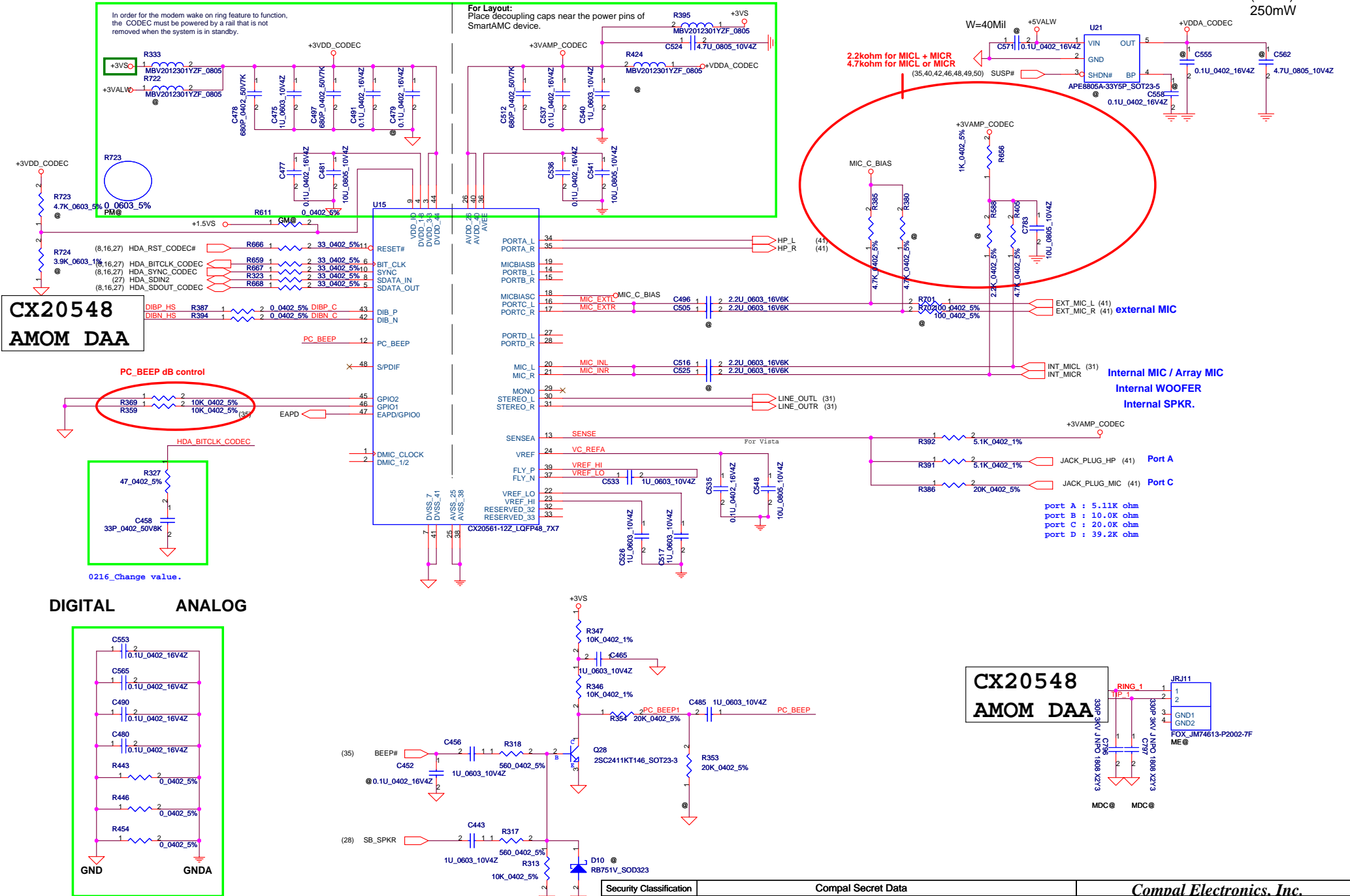


AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680uF, C365 and C368 from 0.1uF to 680p

CODEC POWER

(3.33V)
250mW



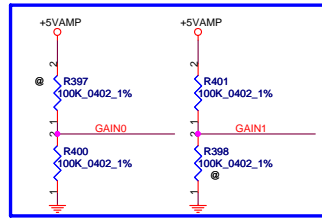
Place these C and R around AGND and DGND, then choose the one which is close to Codec to be accurate.

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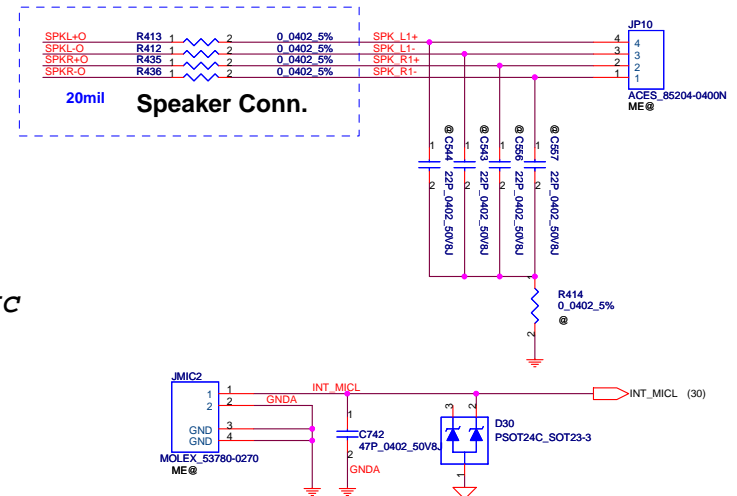
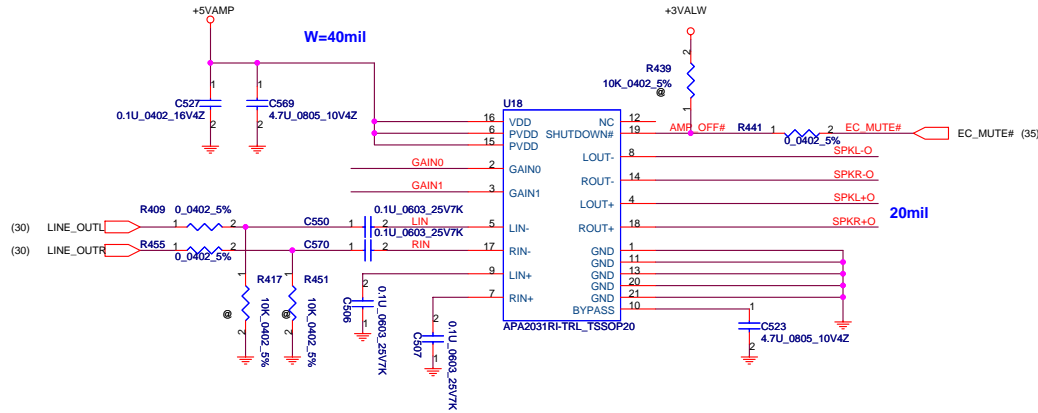
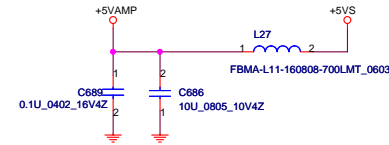
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Size	Document Number	JIWA1/A2_LA-4211P		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	30	of	53

Speaker Amplifier

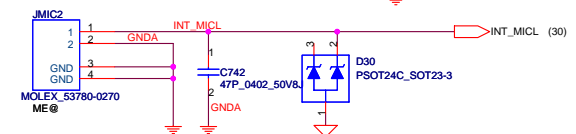
1nd = TPA6017 (SA601720010)
2nd = APA2031 (SA00001RZ00)



GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

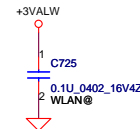
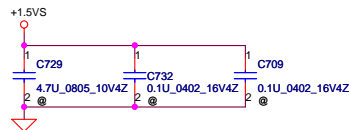
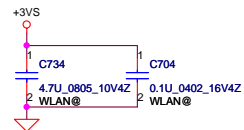


INT MIC

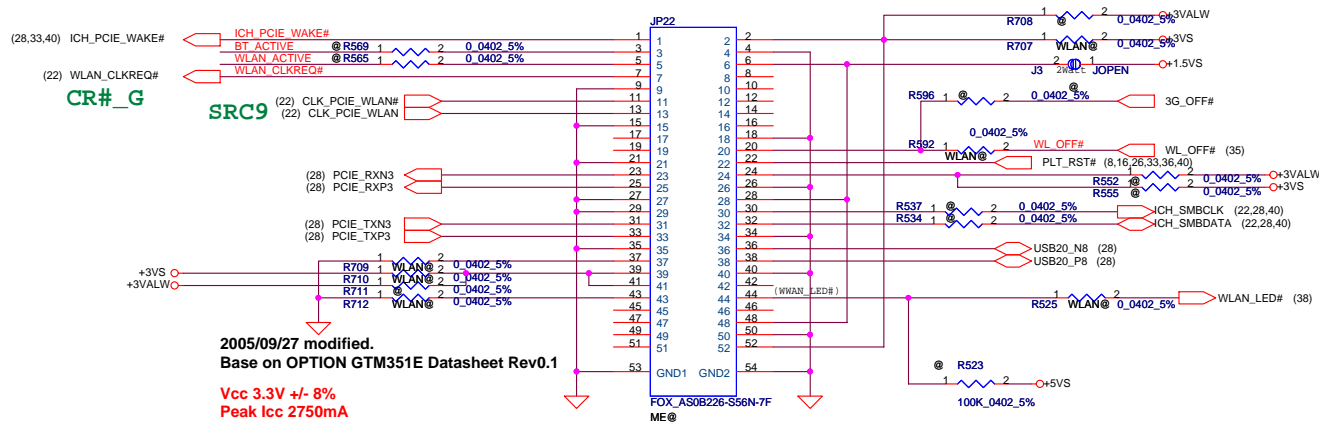


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	AMP/VR/Audio Jack/MIC
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				Document Number JIWA1/A2_LA-4211P
				Rev 1.0
				Date: Monday, May 12, 2008
				Sheet 31 of 53

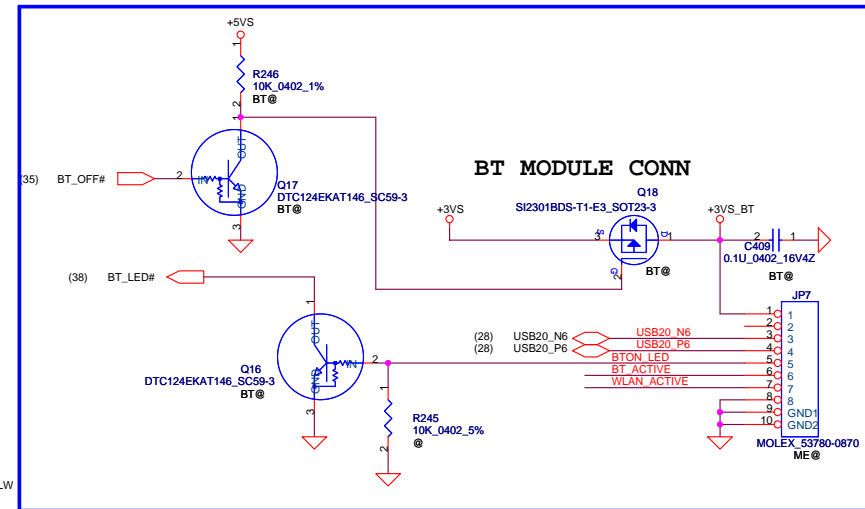
Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN



Mini-Express Card(Slot 1-WLAN)



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



Security Classification		Compal Secret Data		Title	
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Size		Document Number		Rev	
Date		Monday, May 12, 2008		Sheet 32 of 53	

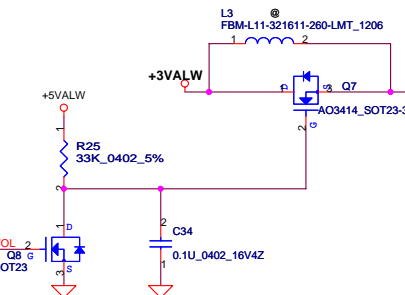
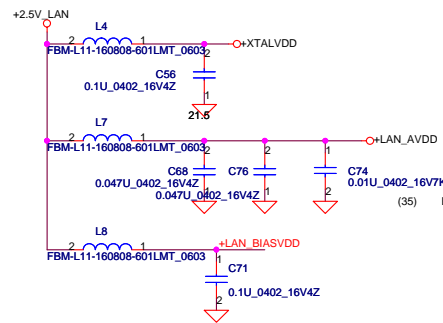
Compal Electronics, Inc.

Mini-Card/3G/FeliCa/BT

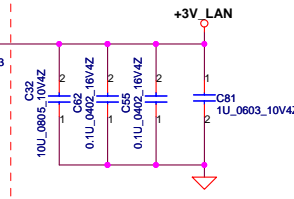
J1WAI/A2_LA-4211P

Rev 1.0

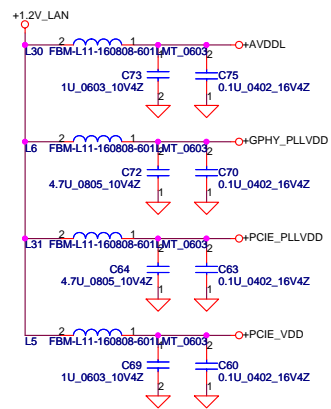
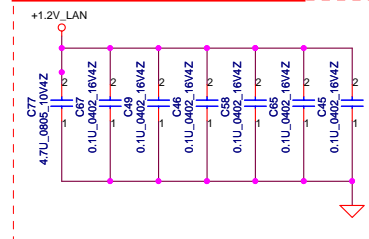
Layout Notice : Filter place as close chip as possible.



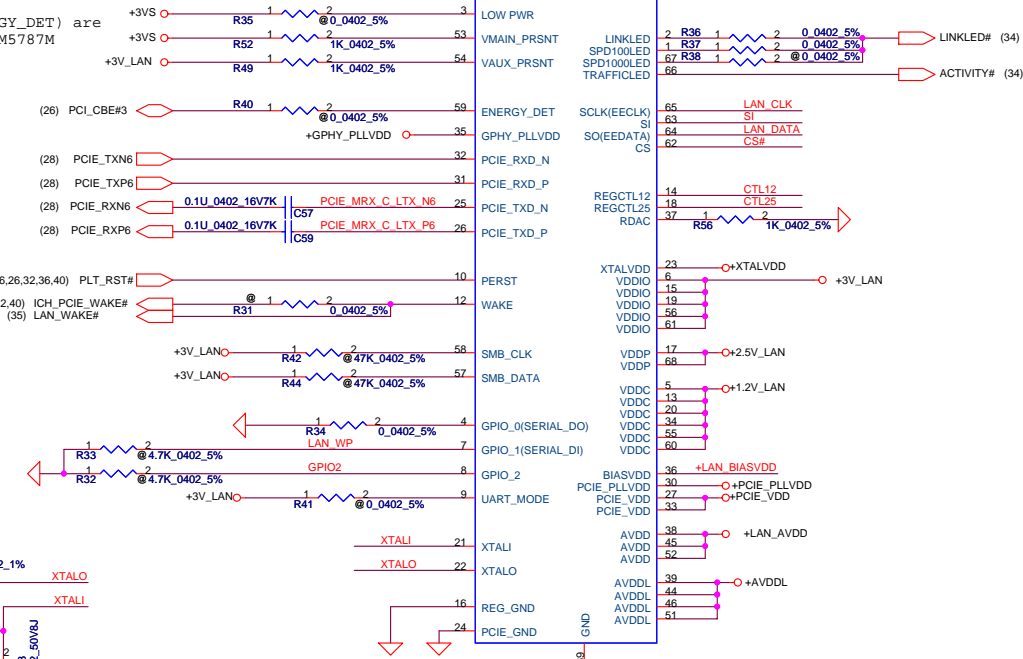
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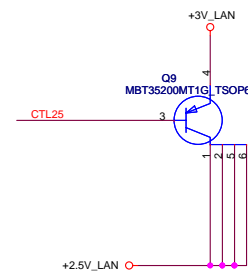
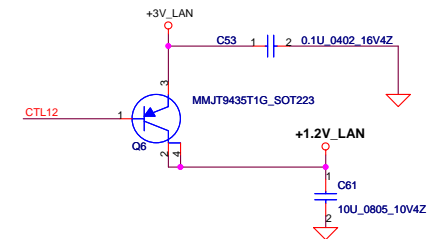
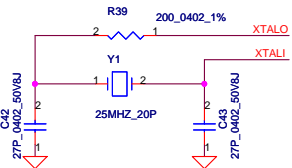
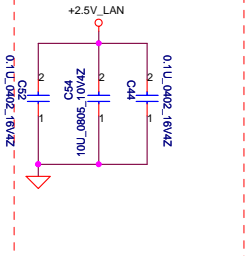
Layout Notice : 1.2V filter. Place as close to chip as possible.



(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

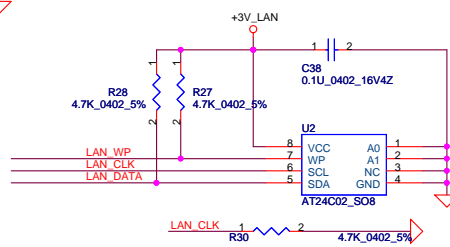


Layout Notice : Place as close chip as possible.



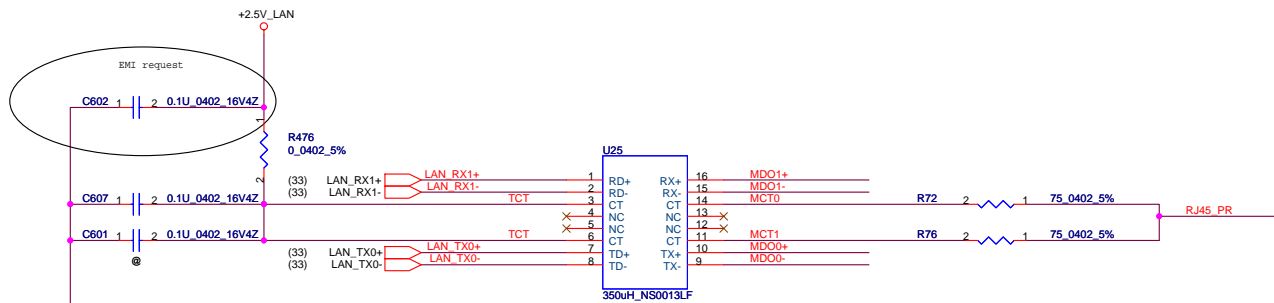
Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close to chip as possible.

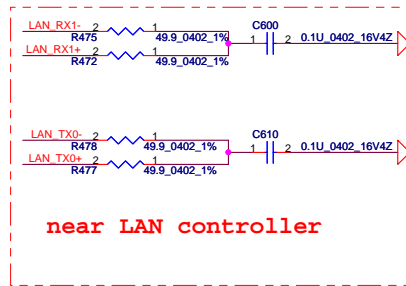


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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				Custom	J1WA1/A2_LA-4211P	1.0
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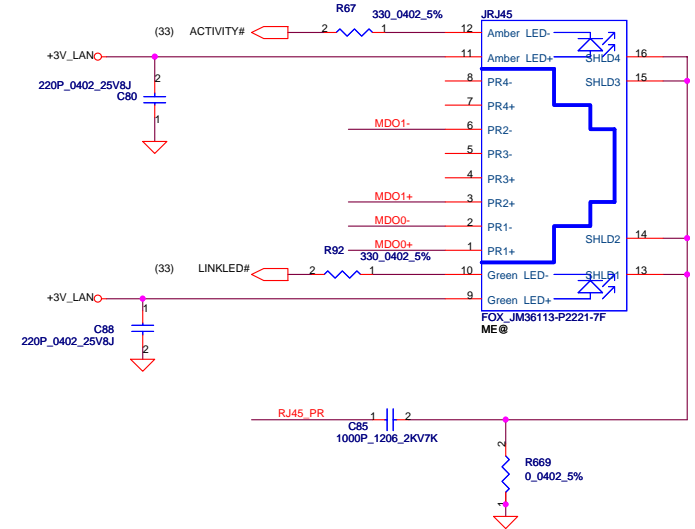
WWW.AliSaler.Com



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



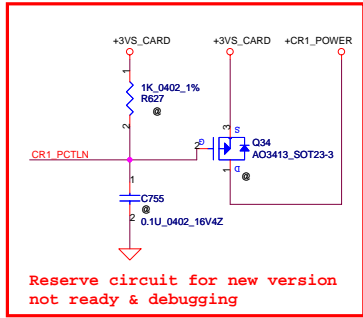
RJ45 CONN



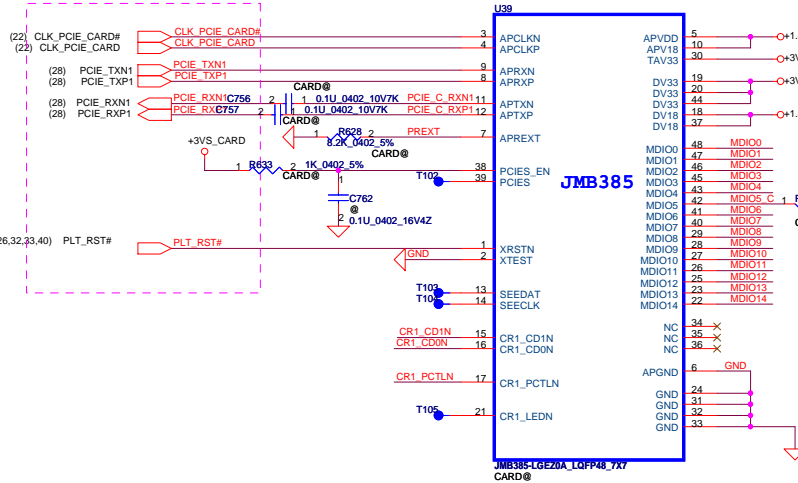
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	LAN CONTROLLER	
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	BIOS & EC I/O Port	
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				Custom	J1WA1/A2 LA-421IP	1.0
				Date: Tuesday, May 20, 2008		

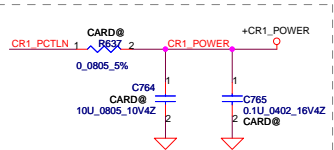
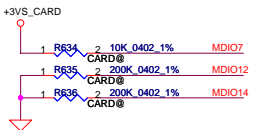
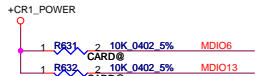


Need check CLK GEN & SB select pin & page



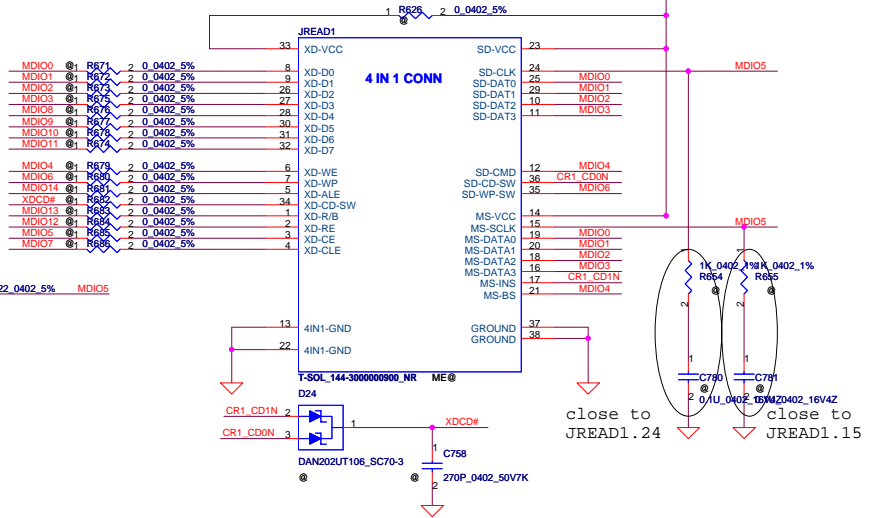
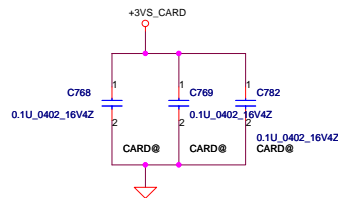
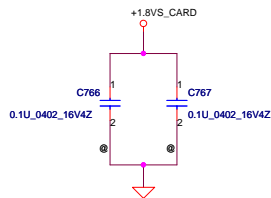
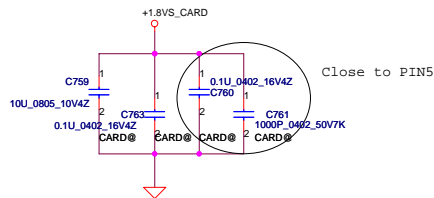
JMB385 Operation Modes

	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X



Use 0805 type and over 20 mils trace width on both side

Card Reader power circuit

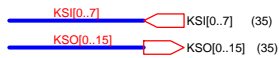


SD,MMC,MS,XD muti-function pin define

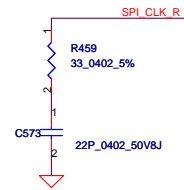
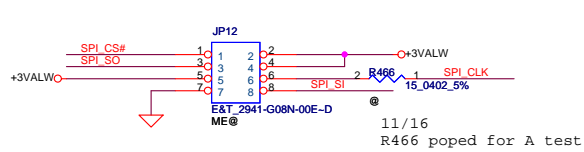
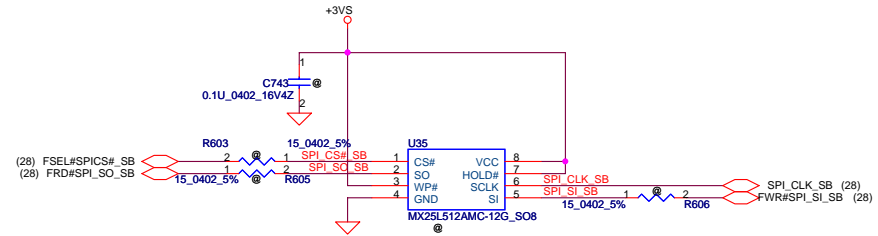
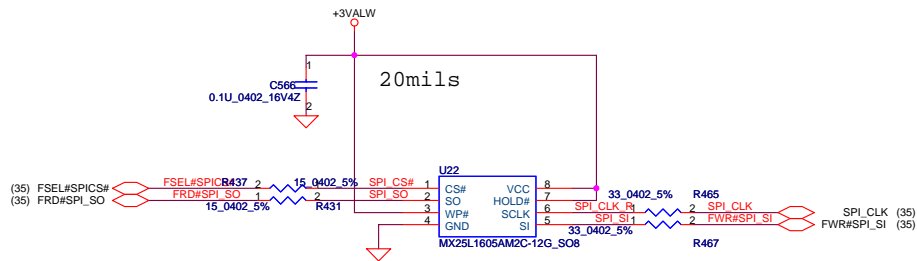
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS Bit 4~7

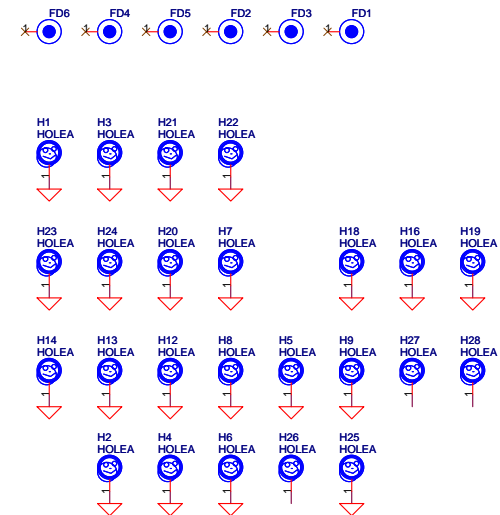
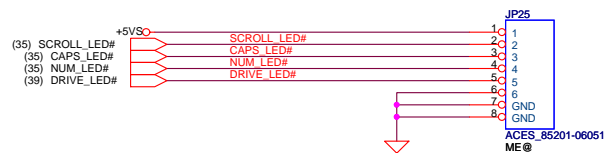
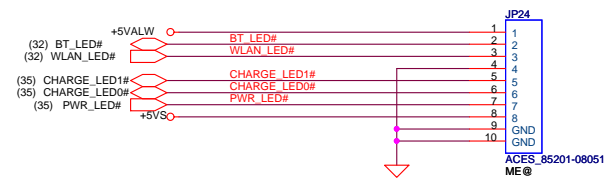
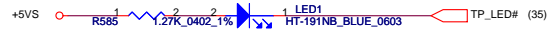
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	4 in 1 Card
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FOR EC 8M SPI ROM

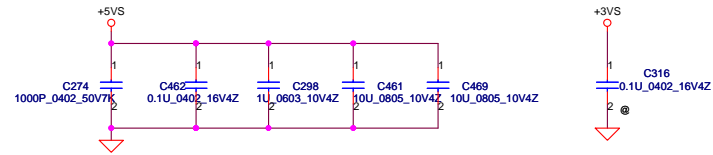


LED

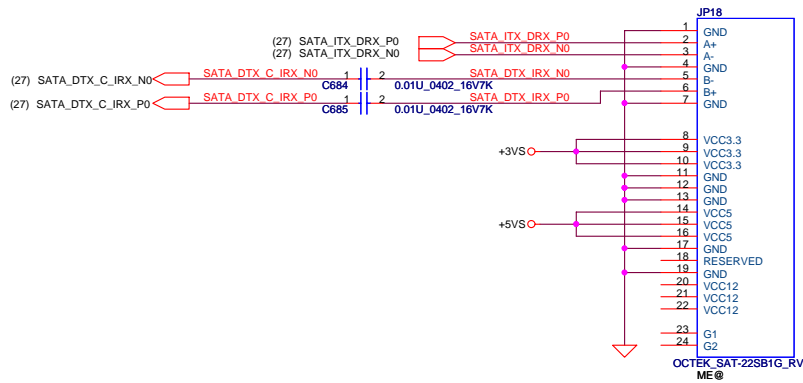


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Issued Date				2007/10/15		Deciphered Date		2008/10/15		Title	
										LED/EC SPI ROM	
										Rev 1.0	
										Date: Wednesday, May 14, 2008	
										Sheet 38 of 53	

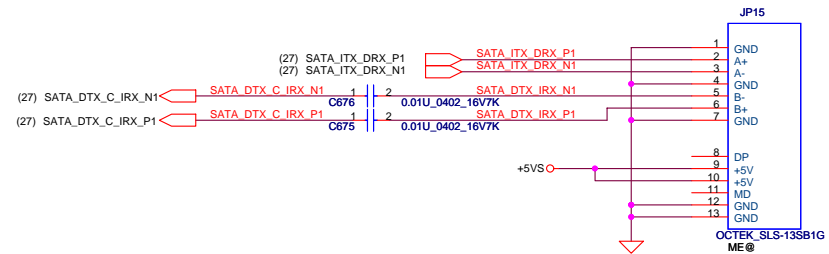
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SATA HDD Conn.

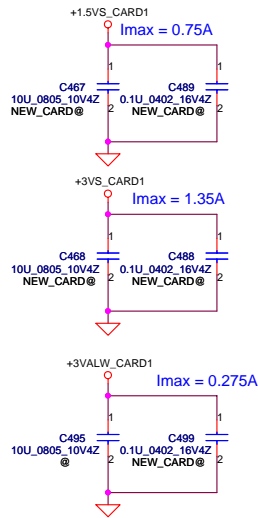
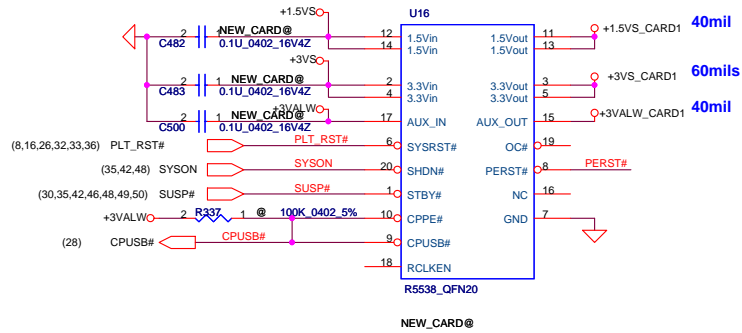


SATA ODD Conn.

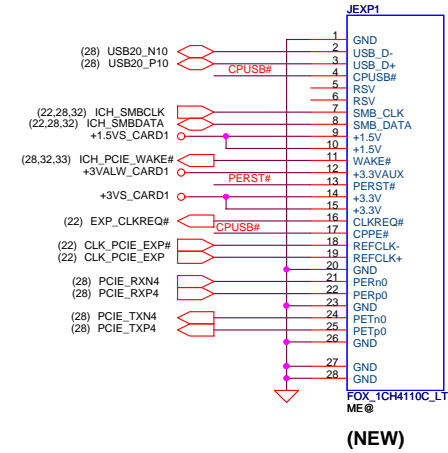


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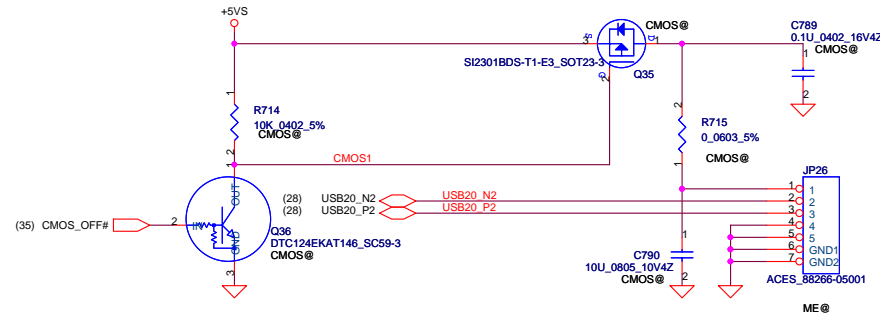
Express Card Power Switch



New Card Socket (Left/TOP)



CMOS Camera Conn



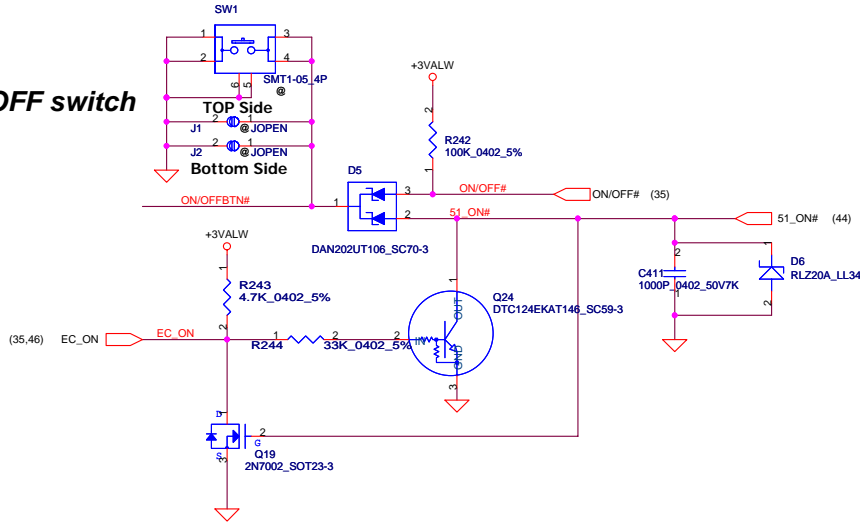
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title		
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NEW CARD & CMOS Connector

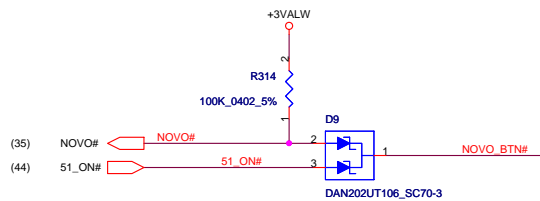
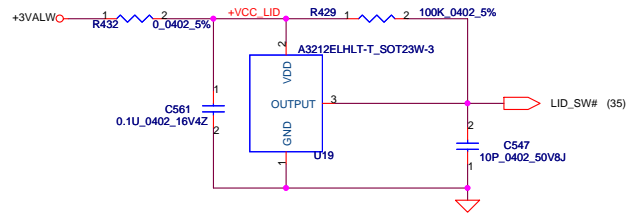
J1WA1/A2_LA-4211P

Power Button

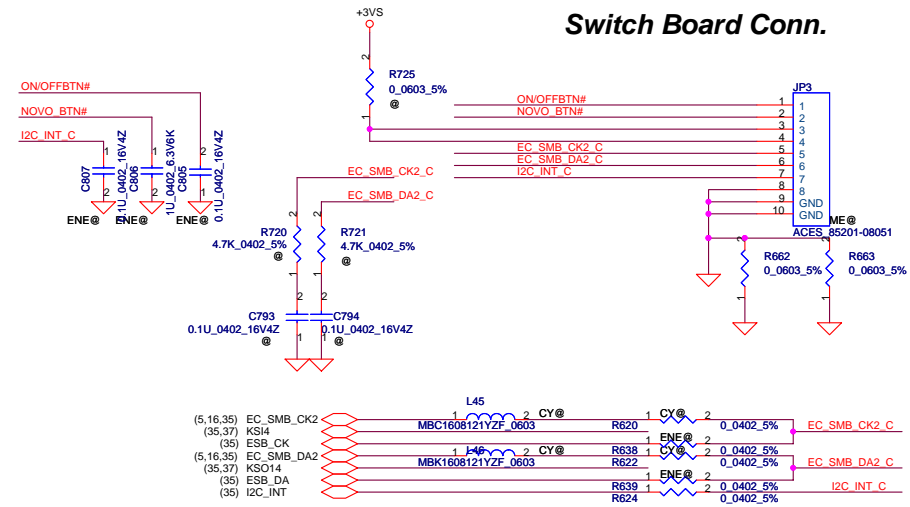
ON/OFF switch



Lid Switch

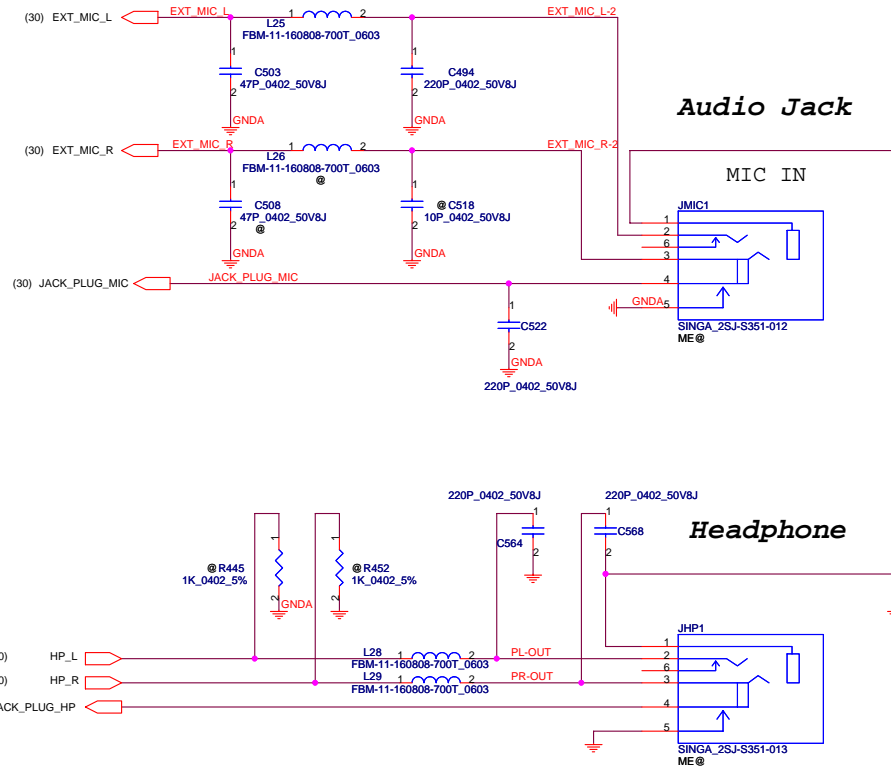


Switch Board Conn.



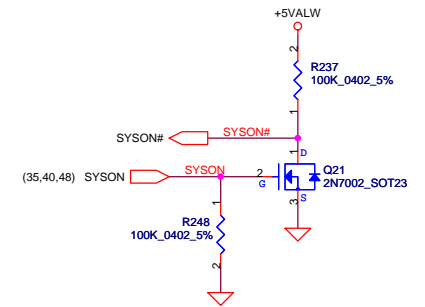
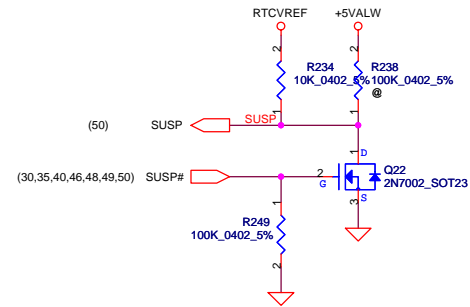
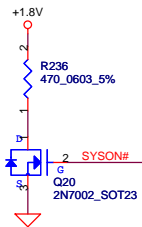
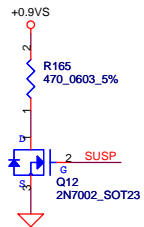
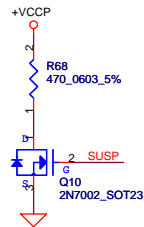
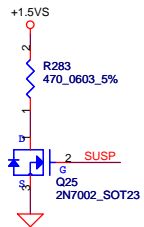
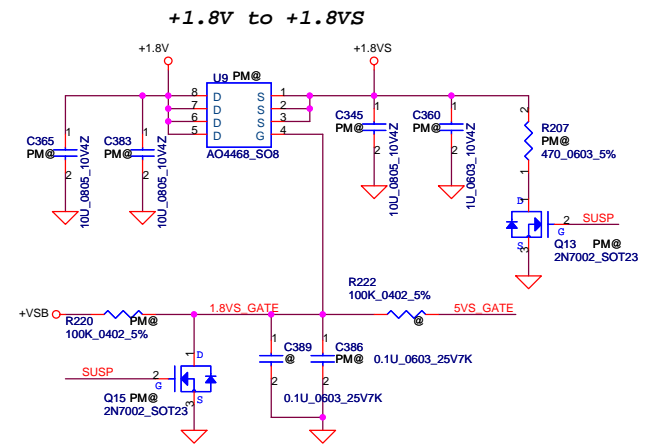
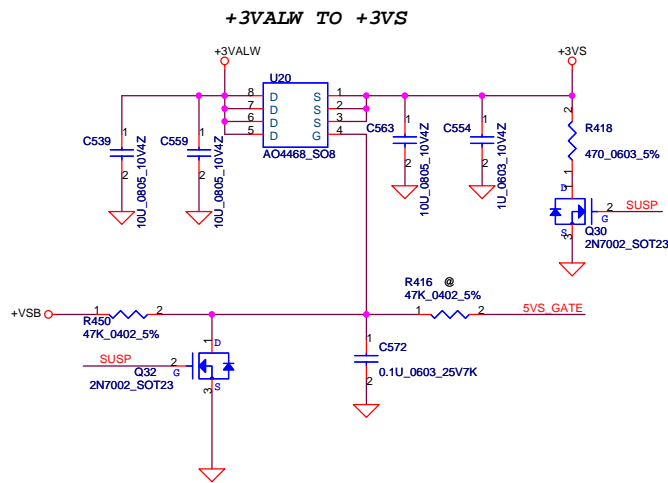
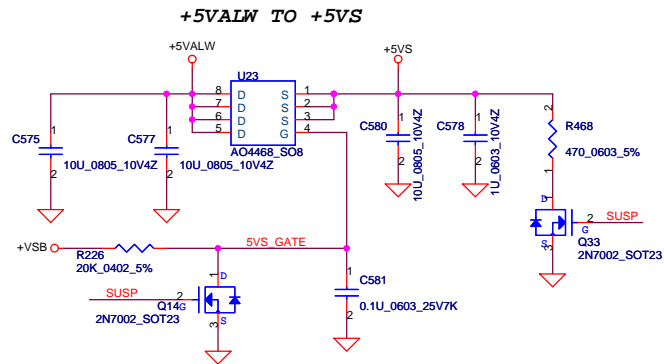
8 mil

Audio Jack

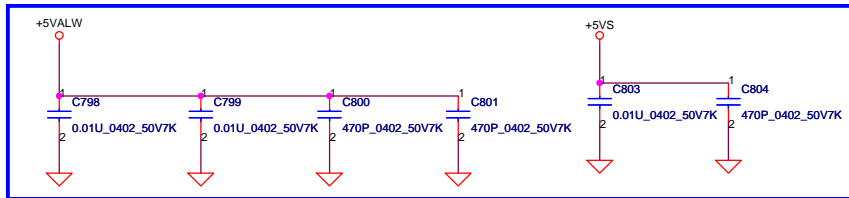


Headphone

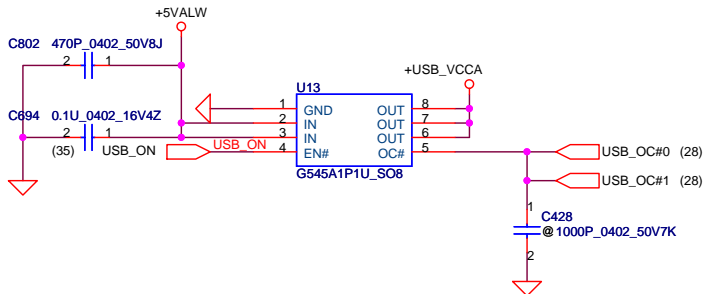
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size B	Document Number	JIWA1/A2_LA-4211P		Rev	1.0
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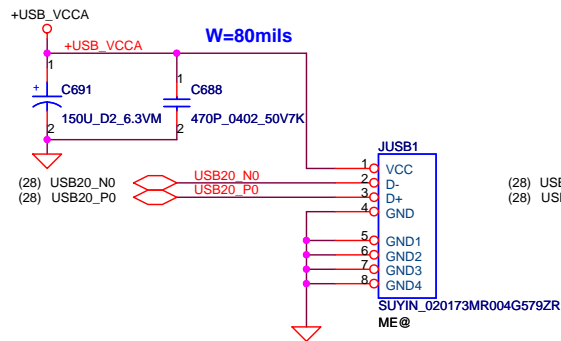
for EMI



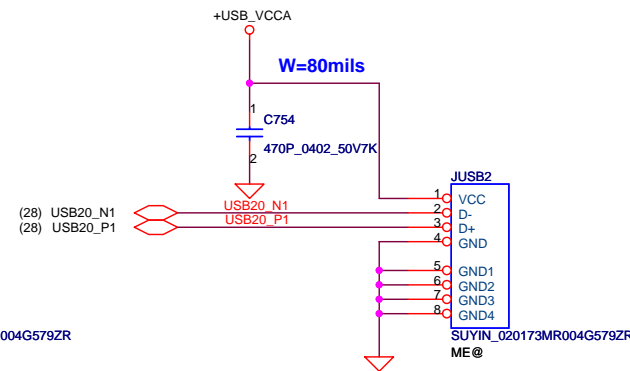
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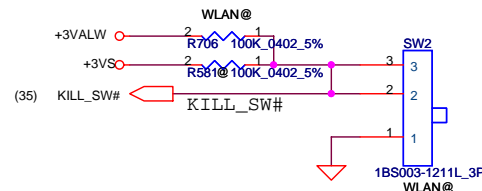
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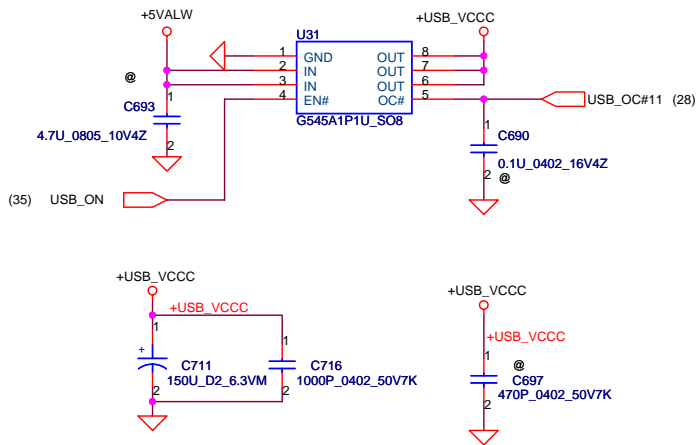
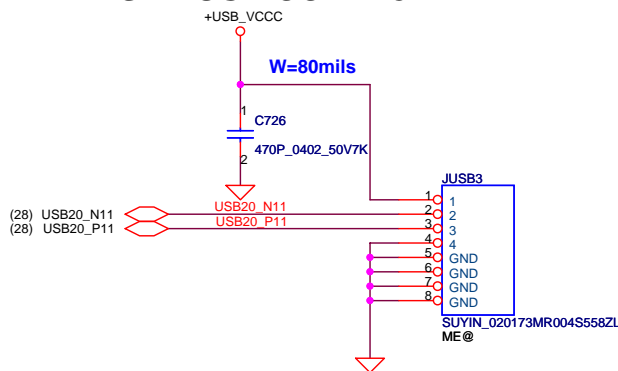
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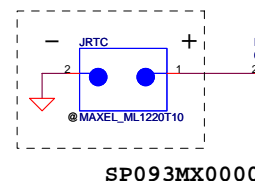
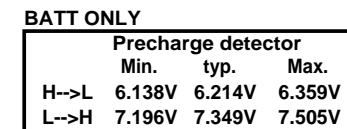
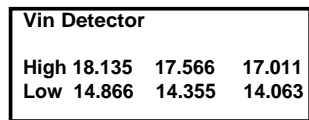
Kill Switch



RIGHT USB CONN. 3

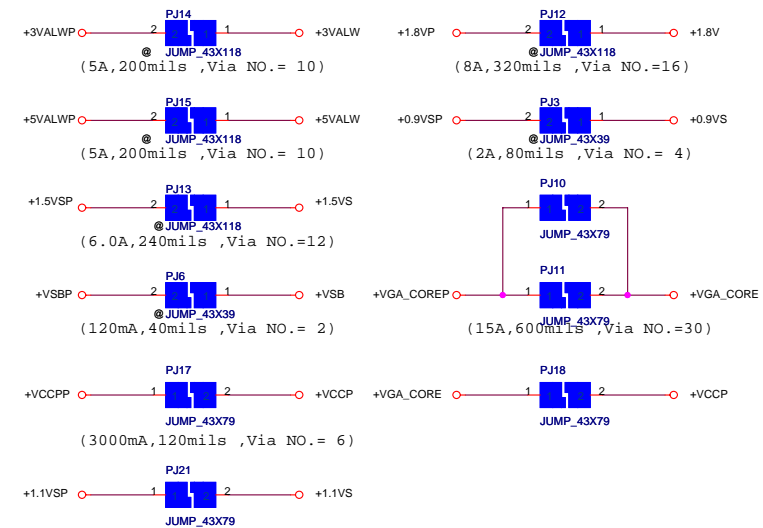
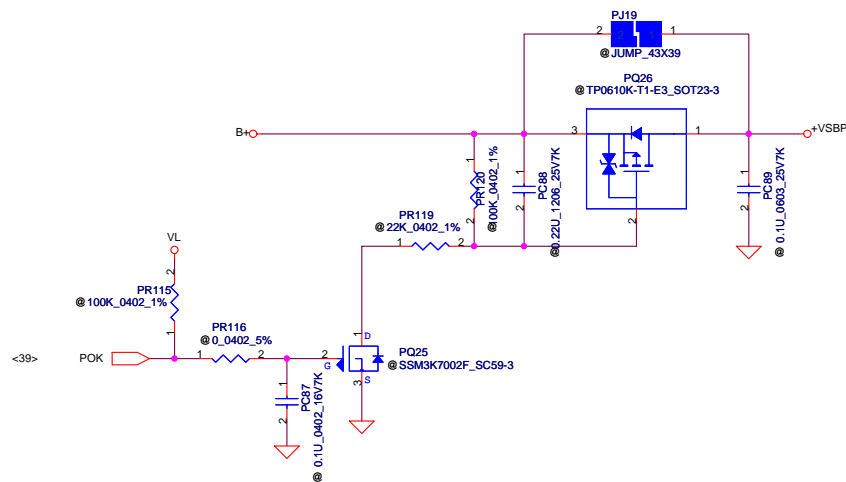
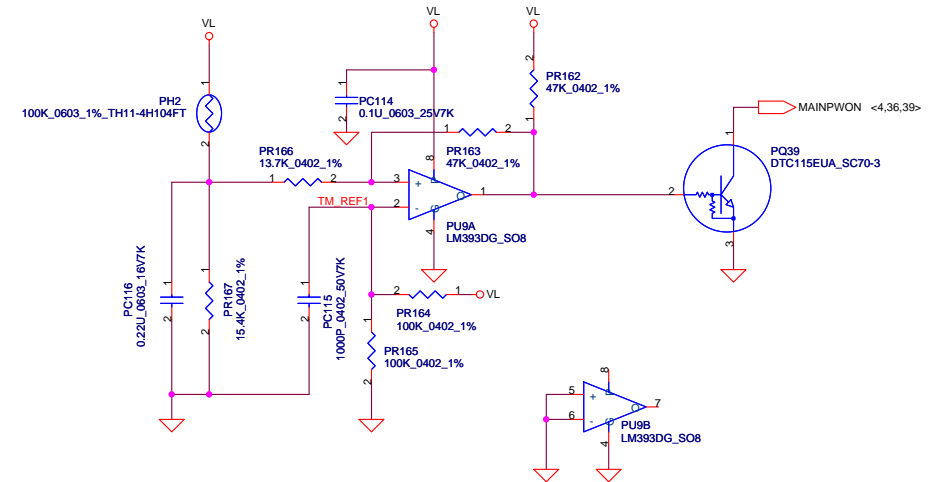
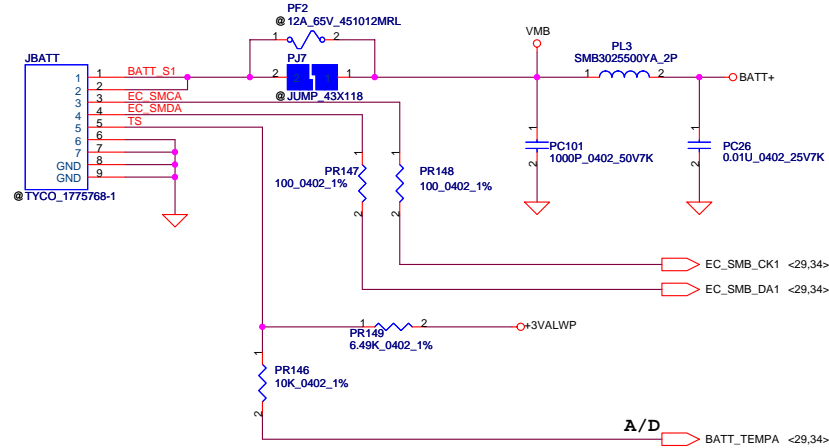


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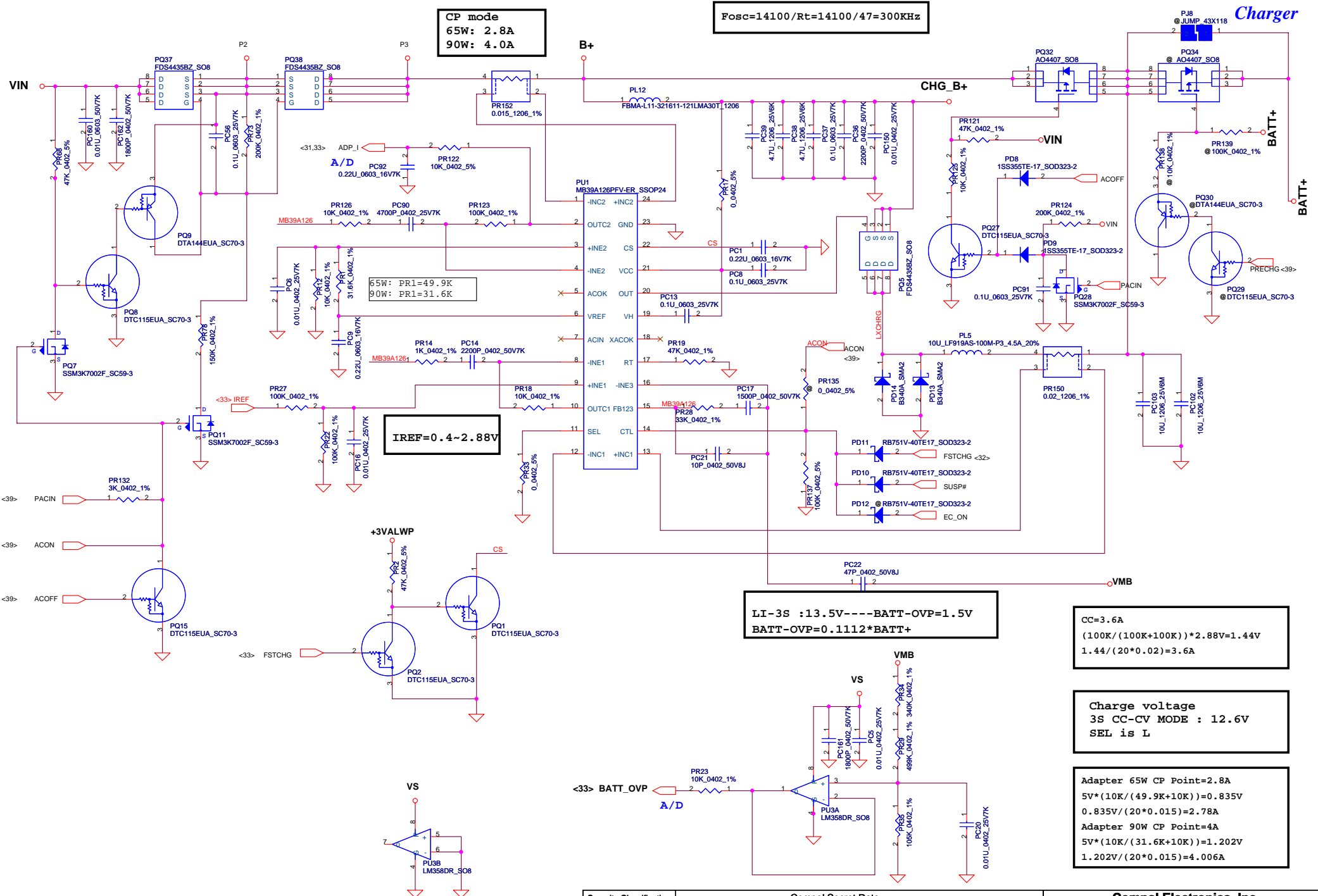


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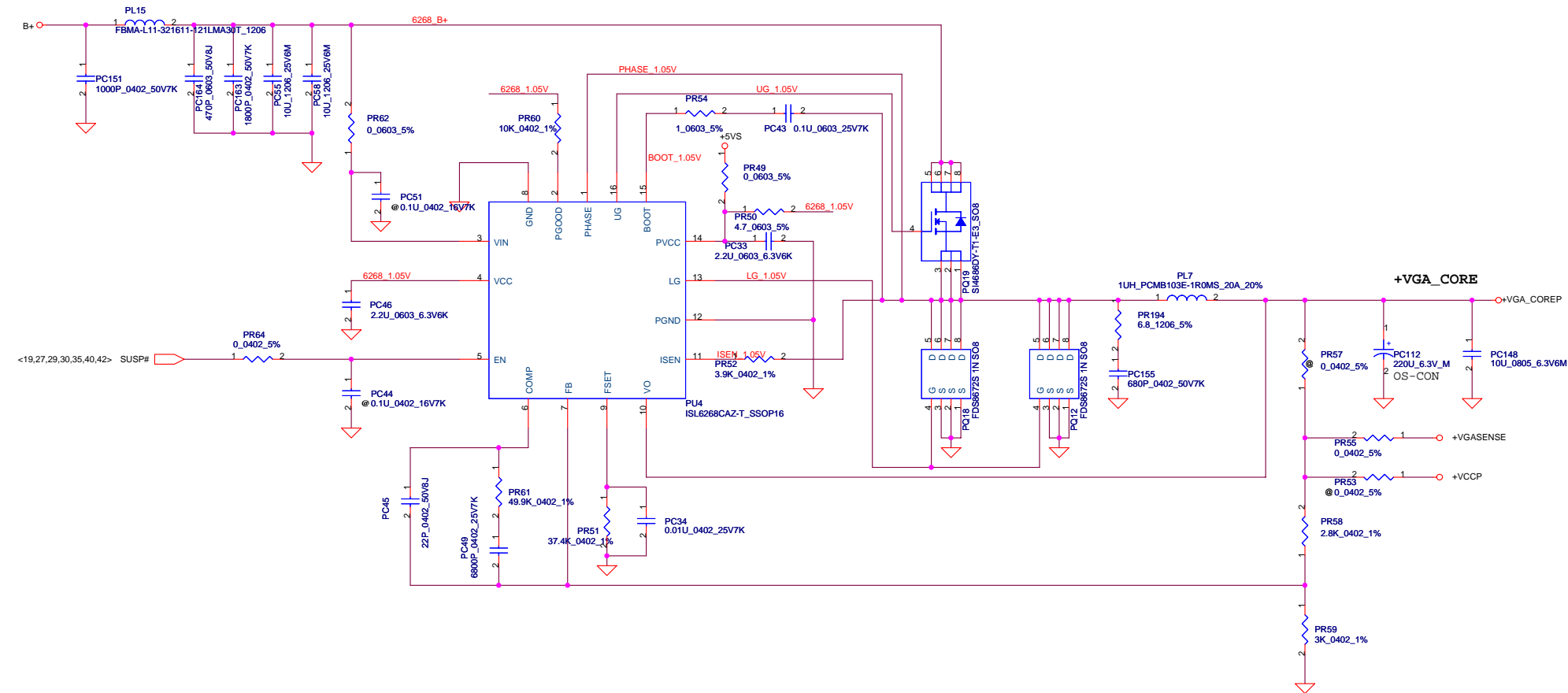
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CPU thermal protection at 92 degree C
Recovery at 56 degree C
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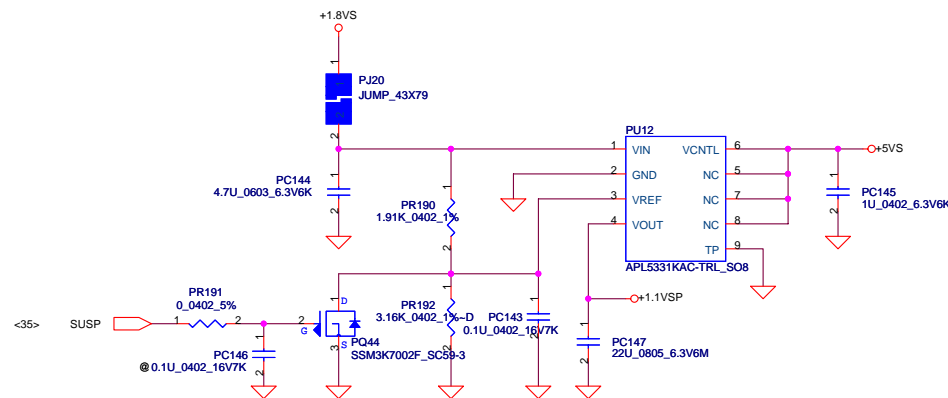
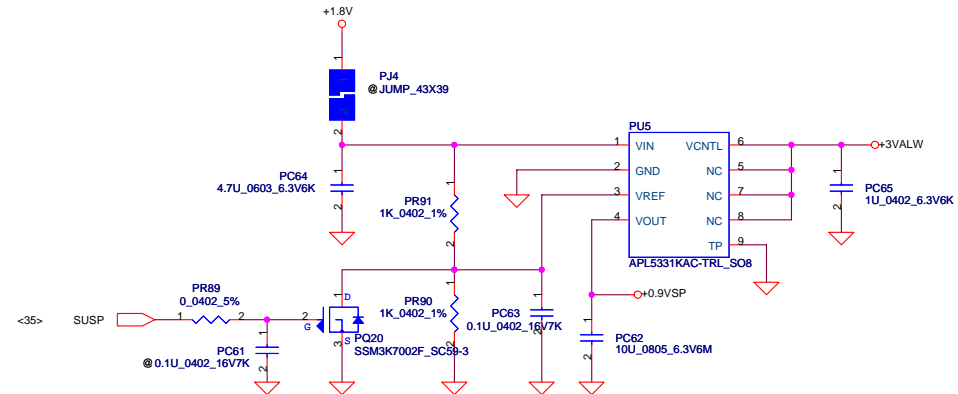
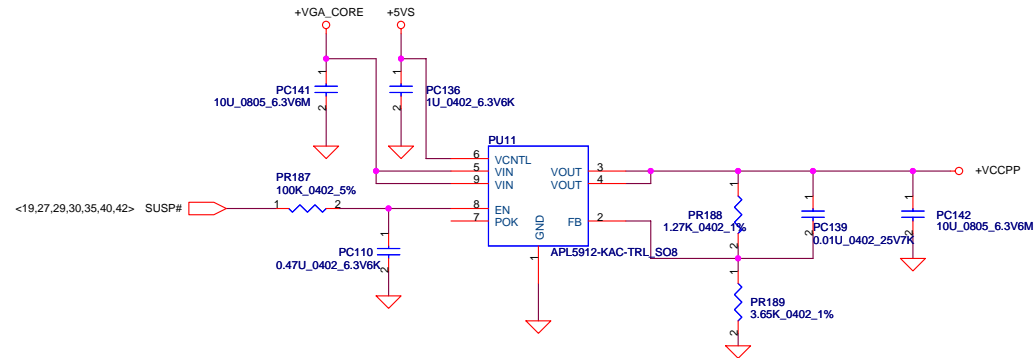
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title BATTERY CONN / OTP		
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										VCCP/0.9V/1.1V	
										Rev	
										1.0	
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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Power PIR

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NO					DATE					PAGE					MODIFICATION LIST					PURPOSE				
1	12/10	P29			C615 change to R615 and BOM Structure change to PM@					Fix DIS Audio issue														
2	12/10	P20、 P21			R104 & R154 BOM Structure change to PM@					Reduce cost														
3	12/10	P16			R86、 R645、 R646、 R650、 R651、 R652 & R653 BOM Structure change to PM@					Reduce cost														
4	12/10	P29			R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm					Fix UMA Audio issue														
5	12/10	P08			R79 change from 33 to 10ohm R80、 R81、 R82 & R85 change from 0 to 22 ohm					Fix UMA Audio issue														
6	12/10	P30			The C783 links to GND					Fix Internal MIC issue														
7	12/10	P41			Add L45 & L46 MBC1608121YZF Bead					Fix F/B issue														
8	01/02	P11			Change C126 package																			
9	01/02	P28			Add R704 to connect VGATE to M_PWROK					Modify power sequence														
10	01/02	P16			Add R699 to connect +VGASENSE																			
11	01/02	P16			Remove U3.P1																			
12	01/02	P16			Add R700 to connect GND																			
13	02/15	P08			Change R147 from 511 ohm 1% to 499 ohm 1%																			
14	02/15	P23			Change D4 location																			
15	02/15	P23			Add D25 & D26 for ESD																			
16	02/15	P25			Add D27、 D28 & D29 for ESD																			
17	02/15	P29			Add R713 connect to 1.5V																			
18	05/08	P05			Add R726 1k ohm & C808 0.1uF to fix issue.																			
19	05/08	P16			Remove R48 for EMI request.																			
20	05/08	P23			Remove HDMI function.																			
21	05/08	P27			Change R554 from 0 ohm to 33 ohm for EMI request.																			
22	05/08	P28			Add R566 10 ohm & C733 10pF for EMI request.																			
23	05/08	P30			Add R327 47 ohm & C458 33pF for EMI request.																			
24	05/08	P35			Change C501 & C514 from 15pF to 12pF																			
25	05/08	P37			Add D31 (PJDLCO5_SOT23-3) for ESD request.																			
26	05/08	P41			Add C494、 C522、 C564 & C568 220pF for EMI request																			

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